EE 330
Lecture 5

Key Historical Developments

Basic Logic Circuits

Review from Last Lecture

Statistics are Real!

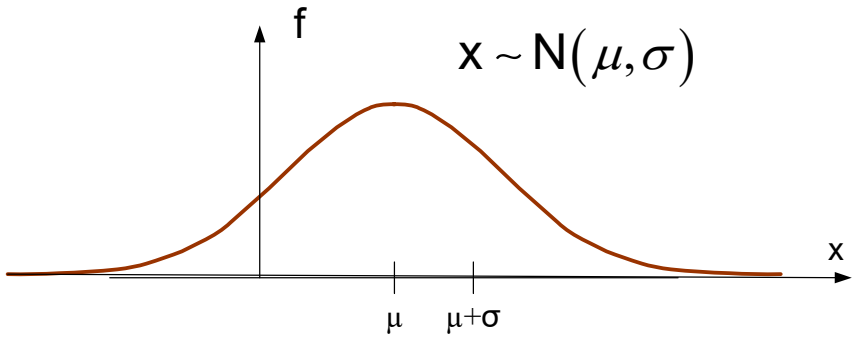
Statistics govern what really happens throughout much of the engineering field!

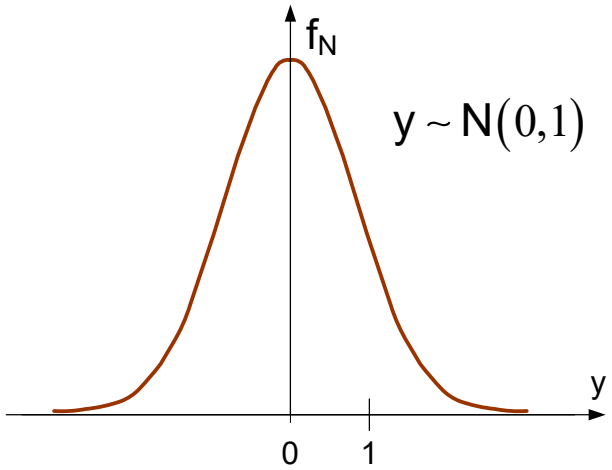
Statistics are your Friend !!!!

You might as well know what will happen since statistics characterize what WILL happen in the presence of variability in many processes !

Review from Last Lecture

Statistics Review





$$\int_{x=-\infty}^{\infty} f(x)\,dx = 1$$

$$y = \frac{x-\mu}{\sigma}$$

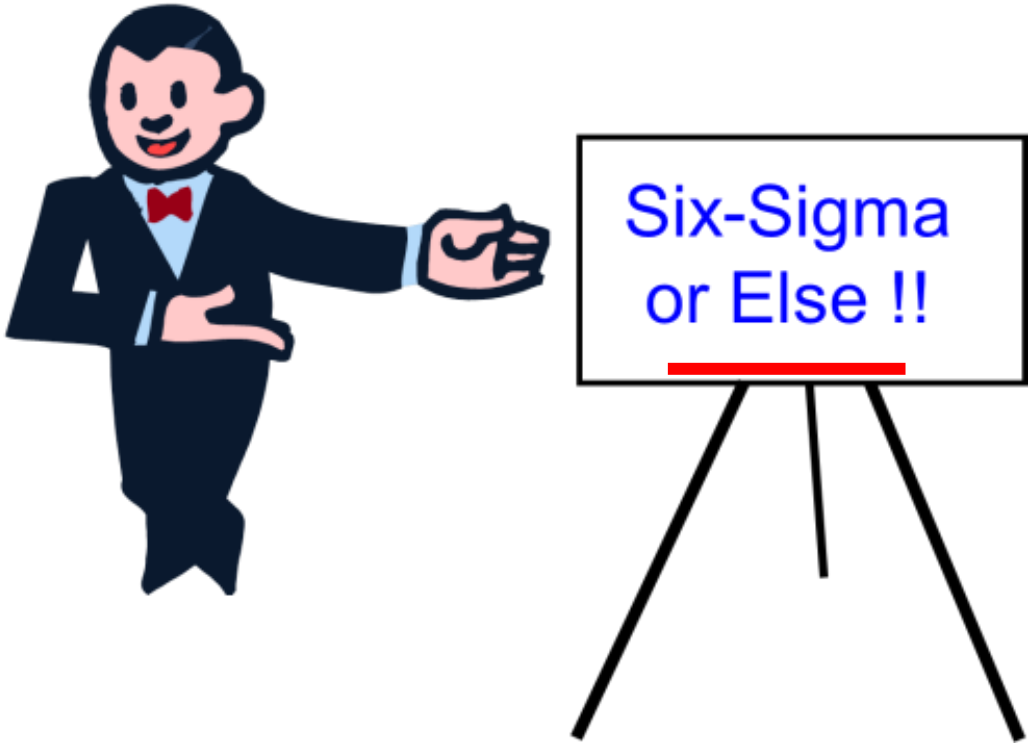
$$\int_{y=-\infty}^{\infty} f_N(y)\,dy = 1$$

Theorem 1: If the random variable x in normally distributed with mean μ and standard deviation σ, then $y = \frac{x-\mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)

Review from Last Lecture

Many Companies Promote the Real Six-Sigma Challenge

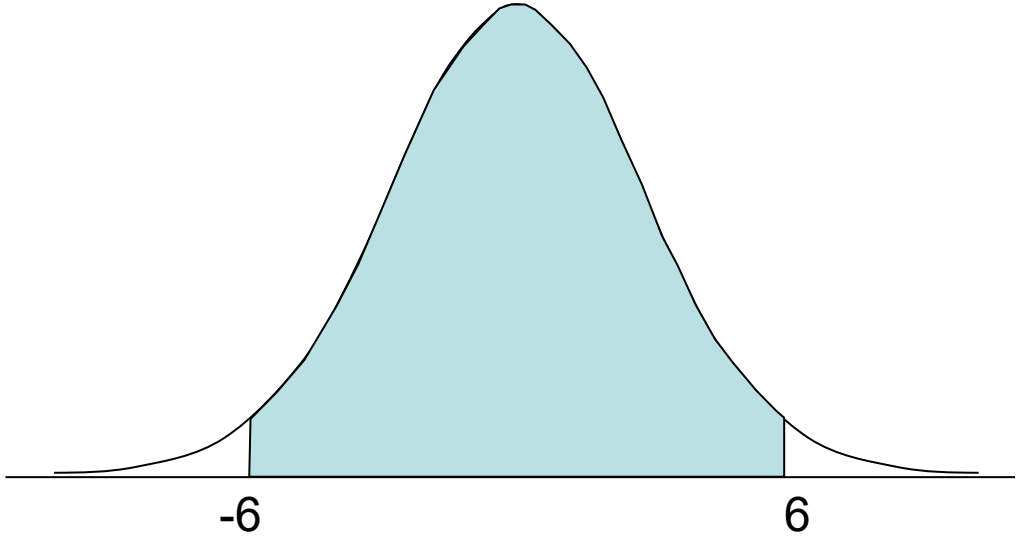


From Wikipedia Sept 1 2021

Six Sigma (**6σ**) is a set of techniques and tools for process improvement. It was introduced by American engineer Bill Smith while working at Motorola in 1986.[1][2] A six sigma process is one in which 99.99966% of all opportunities to produce some feature of a part are statistically expected to be free of defects.

Review from Last Lecture

Yield at the Six-Sigma level



This is approximately 2 defects out of 1 billion parts

Would producing ICs with a yield at the six-sigma level be a good goal?

How about smart phones with defects at this level? (approx. 1.4B sold in 2020)

How about automobiles? (approx. 78 million produced in 2020)

Statistics can be abused !

Many that are not knowledgeable incorrectly use statistics

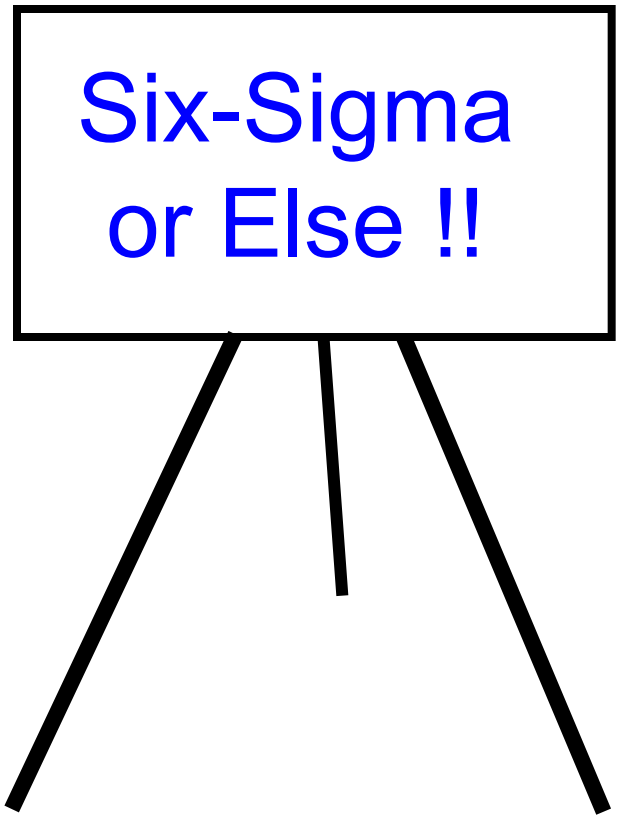
Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics

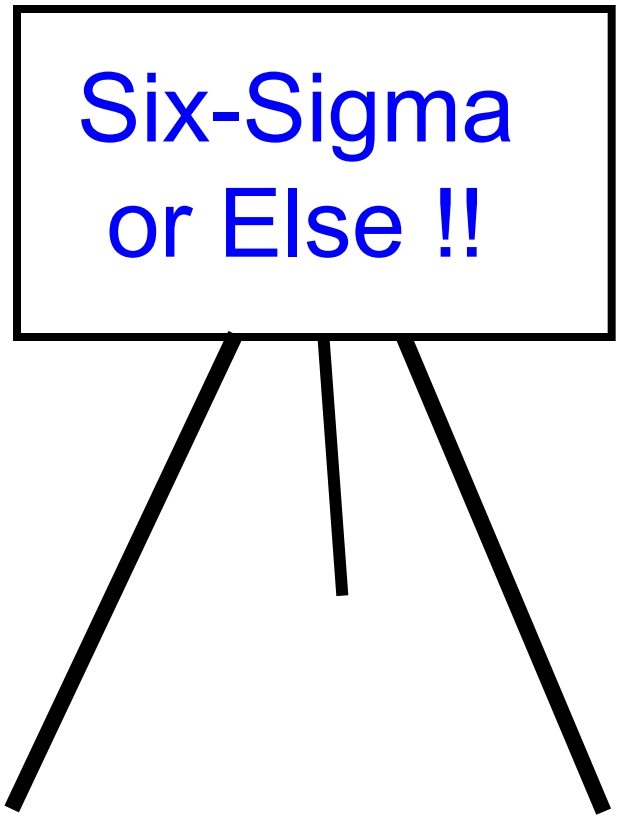
Review from Last Lecture

Meeting the real Six-Sigma Challenge

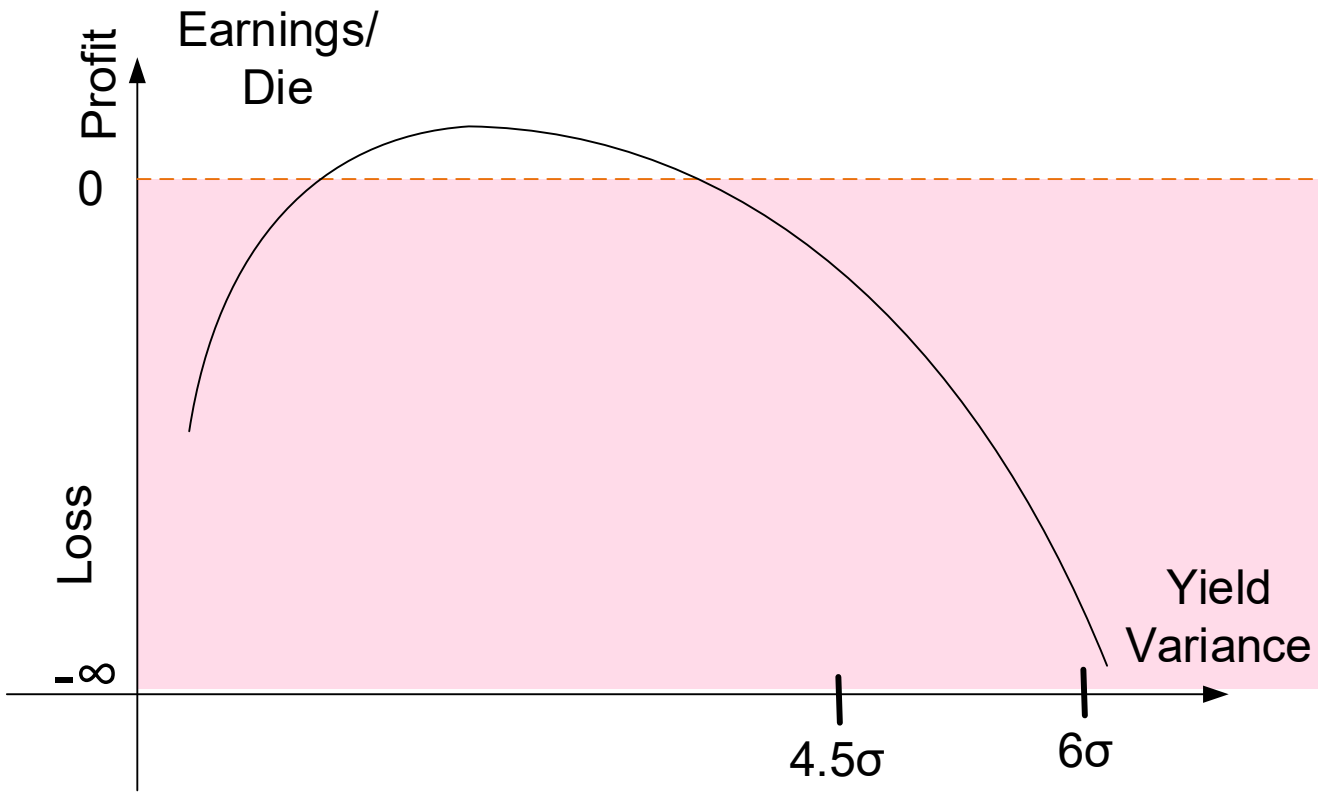


The concept of improving reliability (really profitability) is good – its just the statistics that are abused!

Meeting the real Six-Sigma Challenge



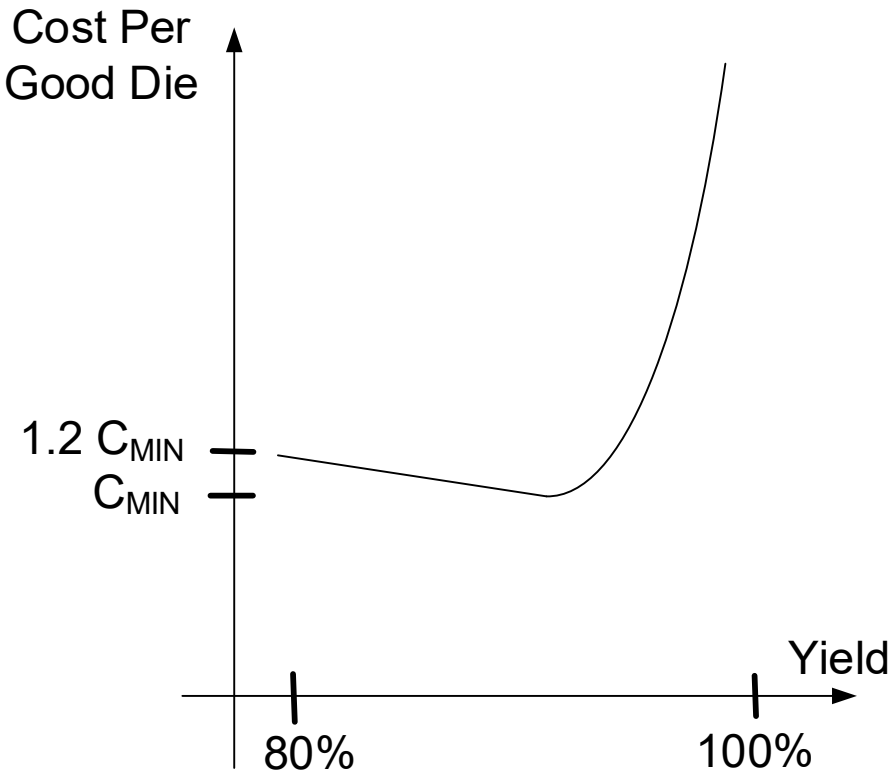
The Reality



- Designing for 4.5σ or 6σ yield variance will almost always guarantee large losses
- Yield targets should be established to optimize earnings not yield variance

Review from Last Lecture

The Reality about Yield



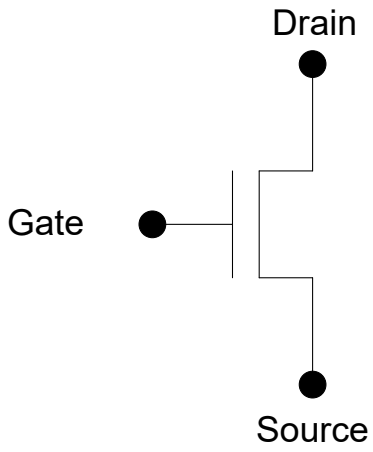
- Return on improving yield when yield is above 95% is small
- Inflection point could be at 99% or higher for some designs but below 50% for others
- Cost/good die will ultimately go to ∞ as yield approaches 100%

Designers goal should be to optimize profit, not an arbitrary yield target

Key Historical Developments

- 1925,1935 Concept of MOS Transistor Proposed (Lilienfield and Heil)
- 1947 BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)
- 1959 Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC
- 1963 Wanless (Fairchild) Experimentally verifies MOS Gate

The MOS Transistor (Field Effect Transistor)



Initially an idea but little more !

1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Julius E. Lilienfeld, passport photo

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode – essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
Lilienfeld, J. E. "Device for controlling electric current," *U. S. Patent No. 1,900,018* (Filed March 28, 1928. Issued March 7, 1933).
Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British Patent No. 439, 457* (Filed March 5, 1935. Issued December 6, 1935).

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

1935 Oskar Heil improved MOSFET

From Wilipedia:

Oskar Heil (20 March 1908, in Langwieden – 15 May 1994, San Mateo, California) was a German electrical engineer and inventor. He studied physics, chemistry, mathematics, and music at the Georg-August University of Göttingen and was awarded his PhD in 1933, for his work on molecular spectroscopy.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
Lilienfeld, J. E. "Device for controlling electric current," *U. S. Patent No. 1,900,018* (Filed March 28, 1928. Issued March 7, 1933).
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https://www.google.com/search?q=Oskar+Heil&biw=1097&bih=568&tbm=isch&imgil=19nt7iXoiQ-X0M%253A%253B8o3VY91vkR5qnM%253Bhttp%25253A%25252F%25252Fwww.avguide.ch%25252Fmagazin%25252Flautsprecher-made-in-ticino-martin-duerrenmatt-perfektioniert-den-heil&source=iu&pf=m&fir=19nt7iXoiQ-X0M%253A%252C8o3VY91vkR5qnM%252C_&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D#imgrc=dv9-icif2DsZ0M%3A&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

Patented Jan. 28, 1930 1,745,175

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

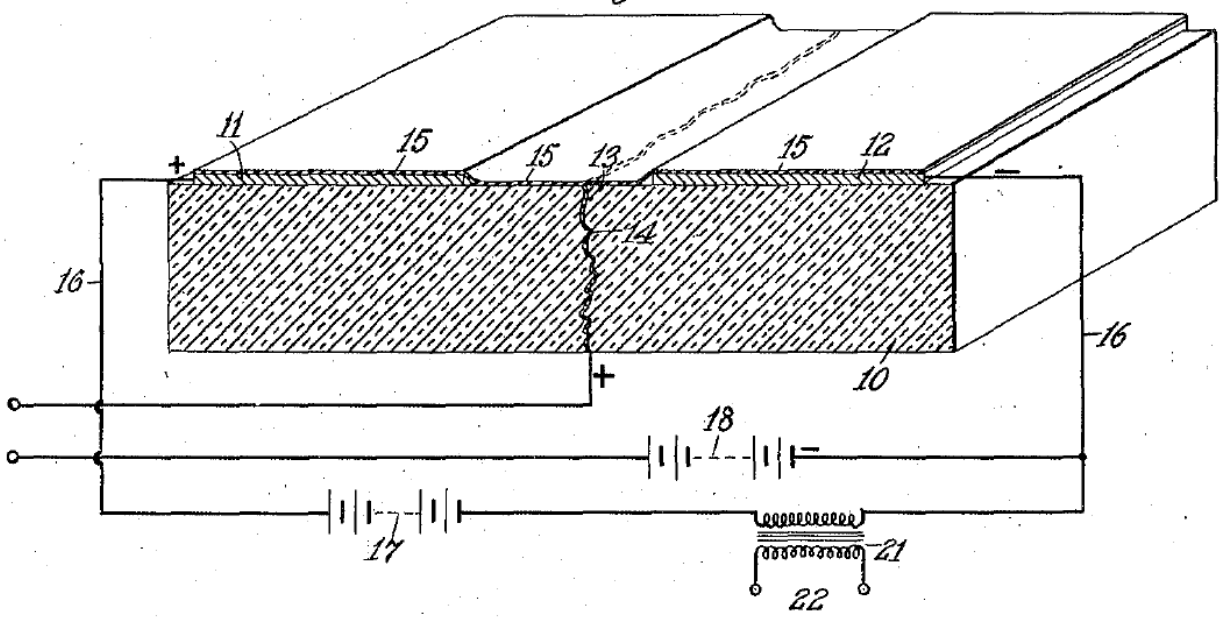
Application filed October 8, 1926, Serial No. 140,363, and in Canada October 22, 1925.

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.



March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

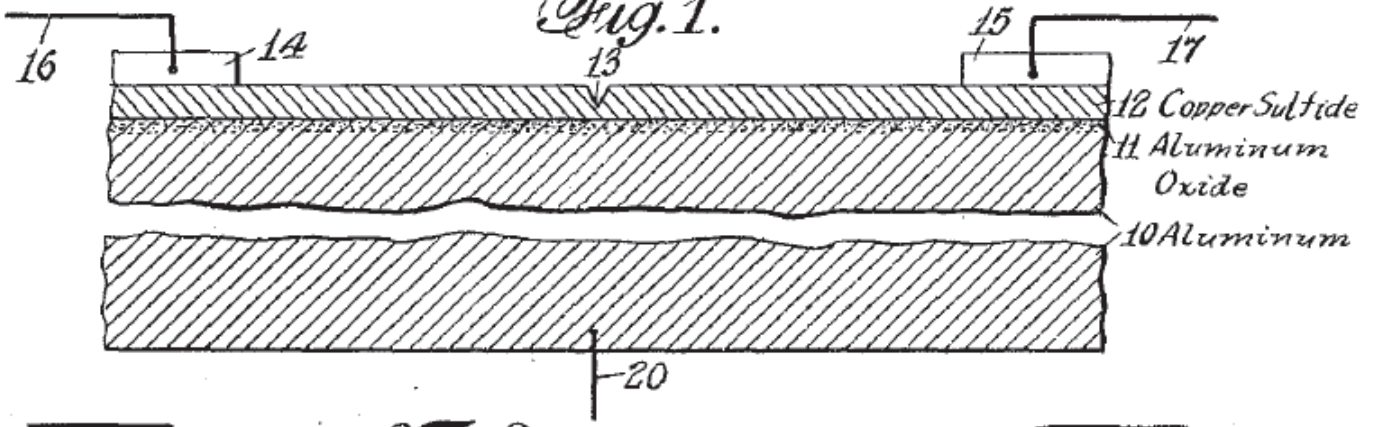
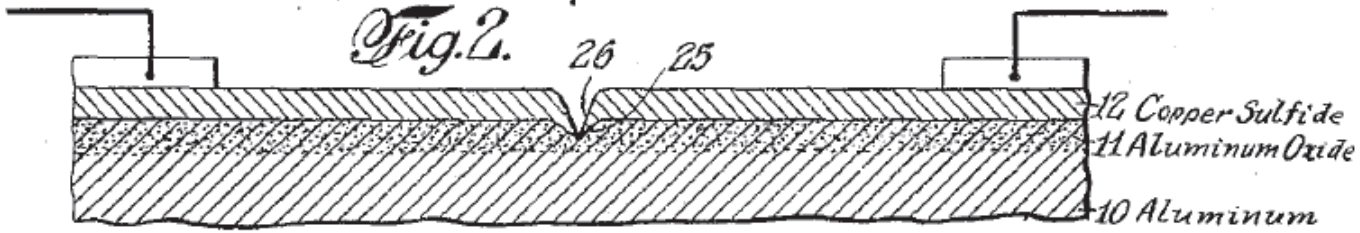


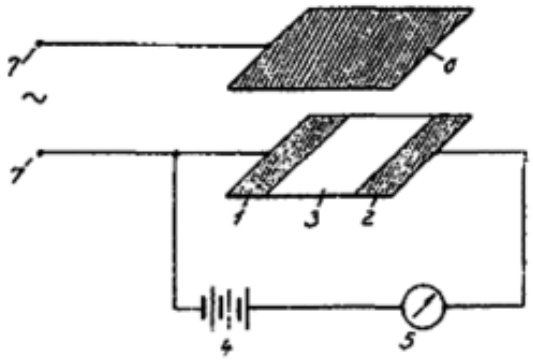
Fig. 2.



Figures from Heil 1935 patent

Insulated gate controls field between other two terminals

Fig. 1



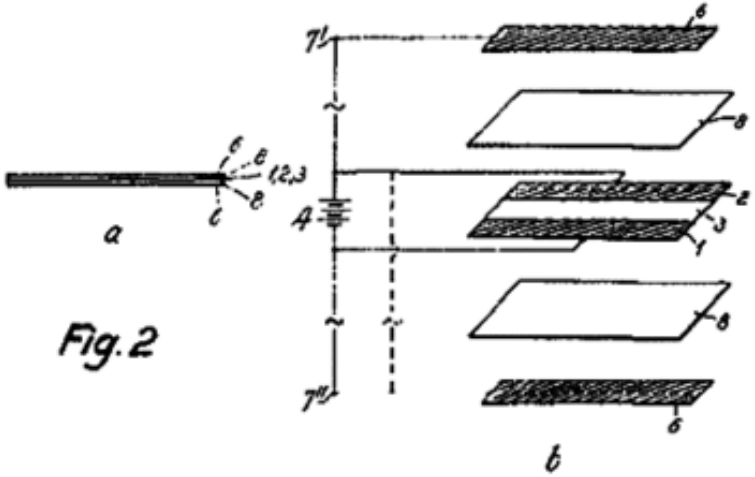
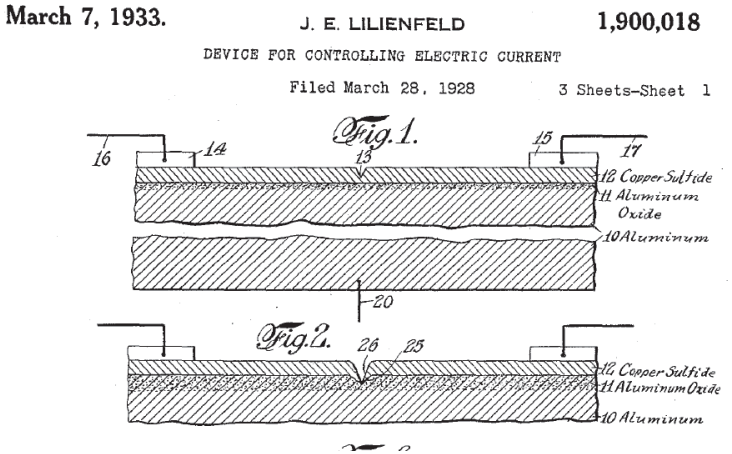


Fig. 2

Though a great idea, of little consequence since couldn't make them!



March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

Fig. 2.

Was there an alternative?

Yes - A relatively new technology – the vacuum tube!

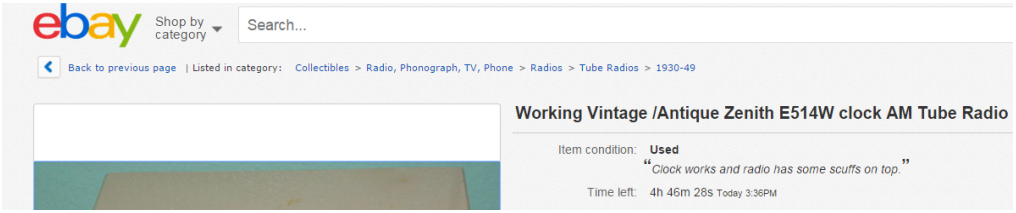
The Vacuum Tube Era

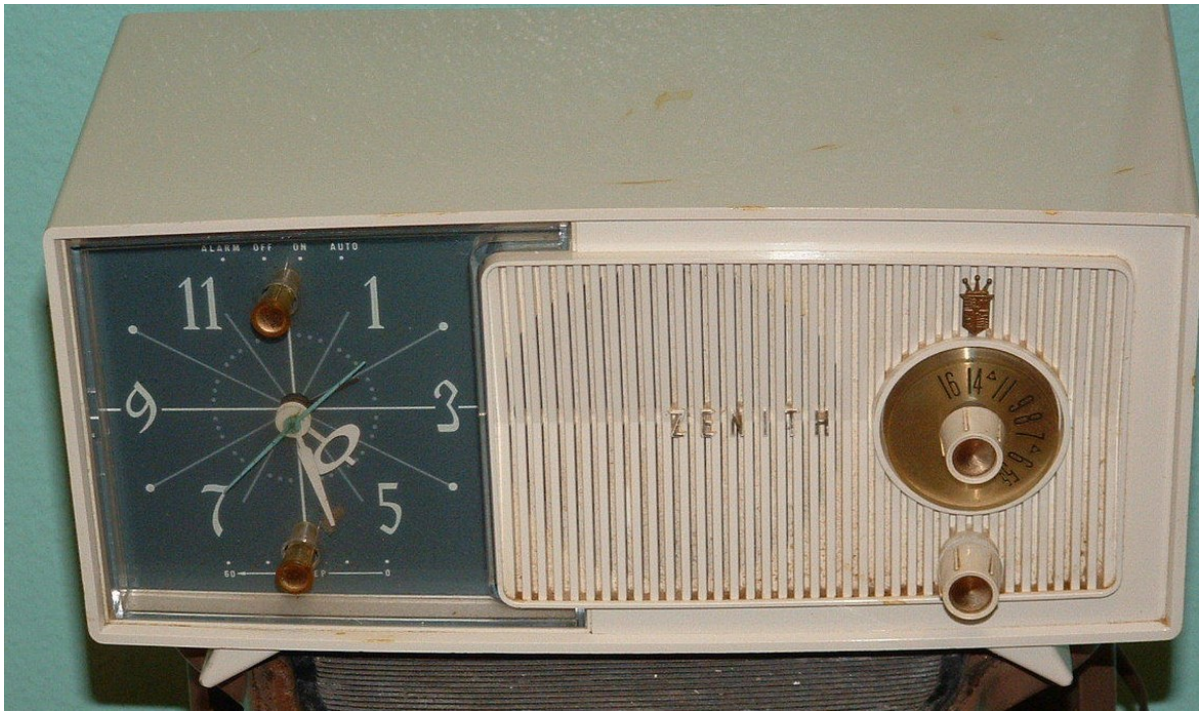
1910 to 1970

The vacuum tube (invented in 1910)

- A major breakthrough in electronics technology
- 6+ decade life span
- Vacuum tube systems not readily affordable by all of society
- Heavy, hot, expensive, large, poor reliability, fragile

The 5-Tube am radio





The 5-Tube am radio

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All American Five

From Wikipedia, the free encyclopedia

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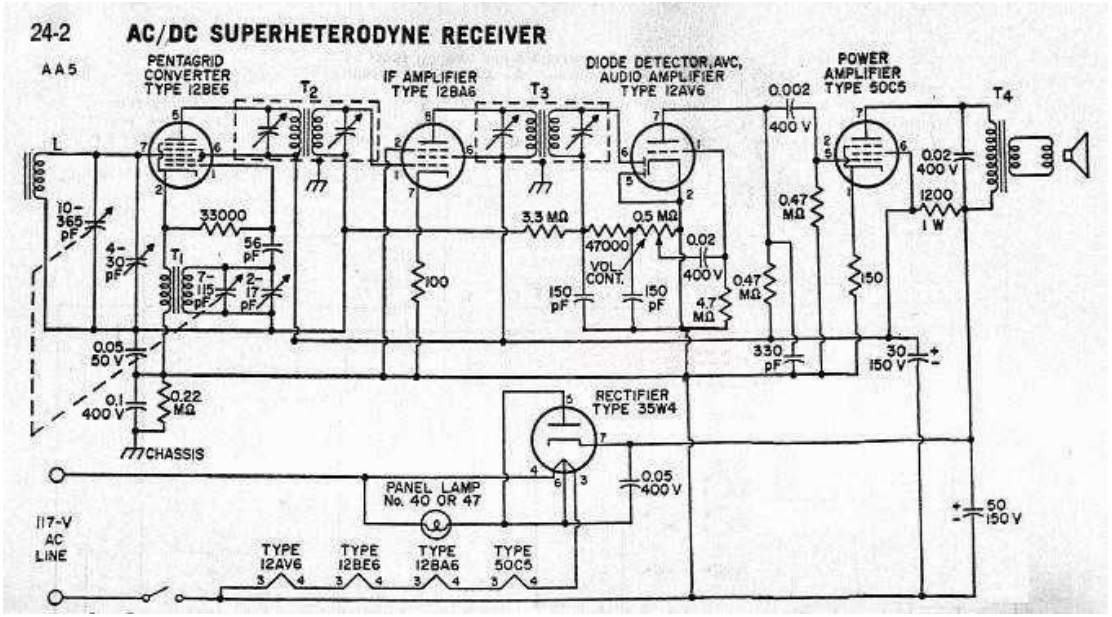
The term **All American Five** is a colloquial name for mass-produced, superheterodyne radio receivers that used five vacuum tubes in their design. These radio sets were designed to receive amplitude modulation (AM) broadcasts in the medium wave band, and were manufactured in the United States from the mid-1930s until the early 1960s[1] By

The 5-Tube am radio

(pictures from WEB pages of images)



Schematics were simple !!

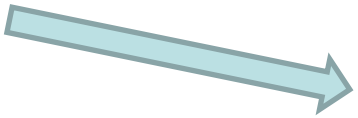
The Vacuum Tube Era

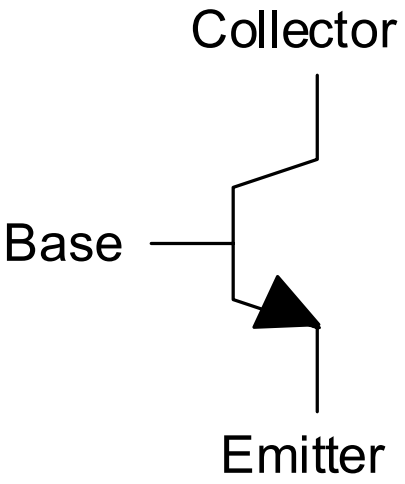
Lots of people supported the industry (primarily radio, later radio and TV) with repair shops throughout the country

(pictures from WEB pages of companies)

Tubes as well as resistors and capacitors had poor reliability

The Bipolar Transistor (Bipolar Junction Transistor – BJT)





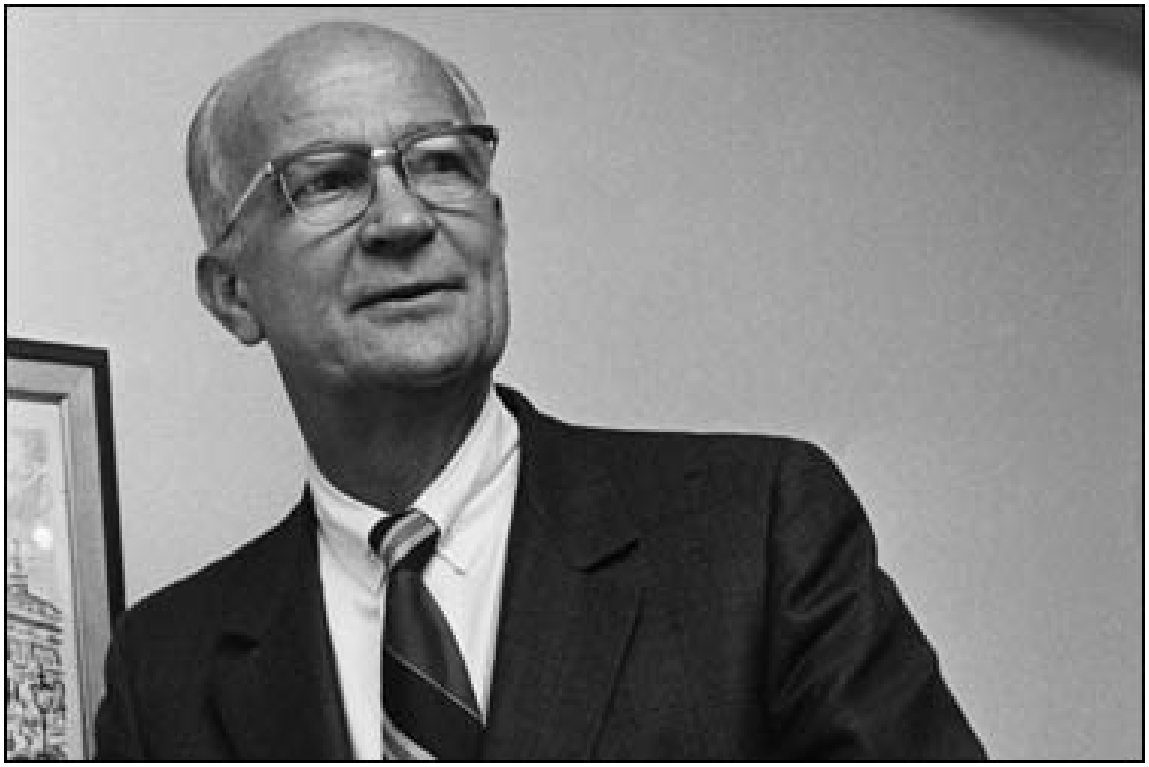
Late 1947

A solution to a major bottleneck limiting the development of electronics technology !

Naming the Transistor

From the group at Bell Labs

"We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances."



William Shockley

http://www.time.com/time/time100/scientist/profile/shockley03.html

William Shockley

He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

Gordon Moore

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.

Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

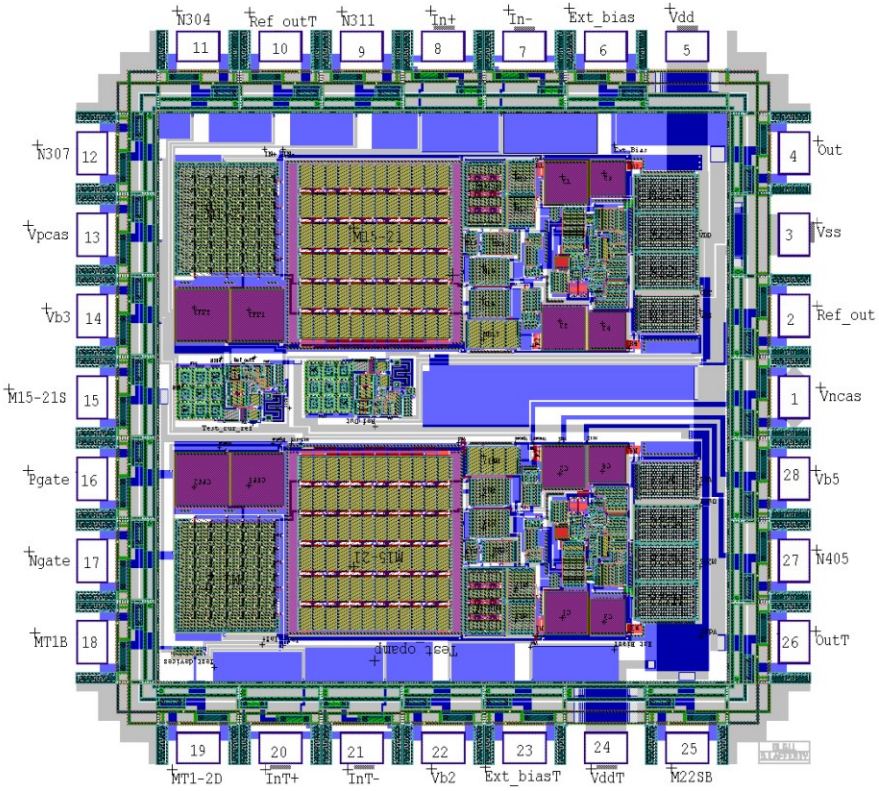
…. (in early 1957 a group of the key people involved with Shockley left and formed a new company named Fairchild Semiconductor …) This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

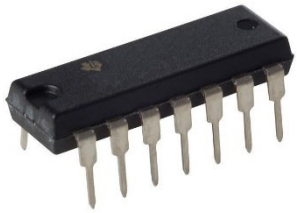
Editor's note:

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

(Fairchild was formed in 1957 – Moore and Noyce were 2 of 8 co-founders)

The Integrated Circuit





June 23, 1964 J. S. KILBY 3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

Filed Feb. 6, 1959 4 Sheets-Sheet 1

Fig. 1.

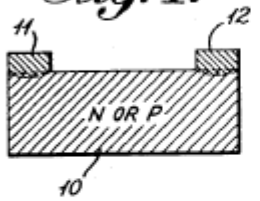


Fig. 1a.

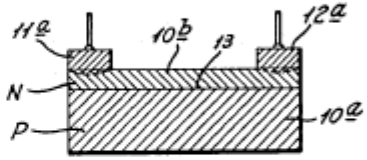


Fig. 2.

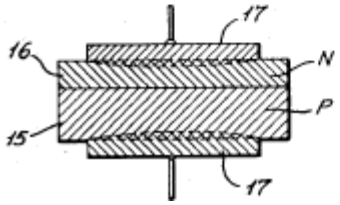


Fig. 2a.

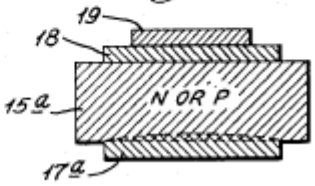


Fig. 5.

June 23, 1964 J. S. KILBY 3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

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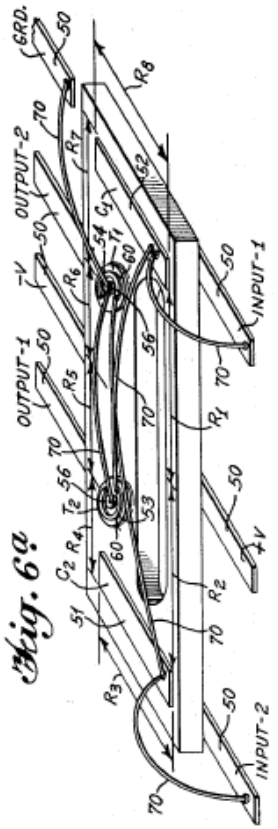

Fig. 6a.

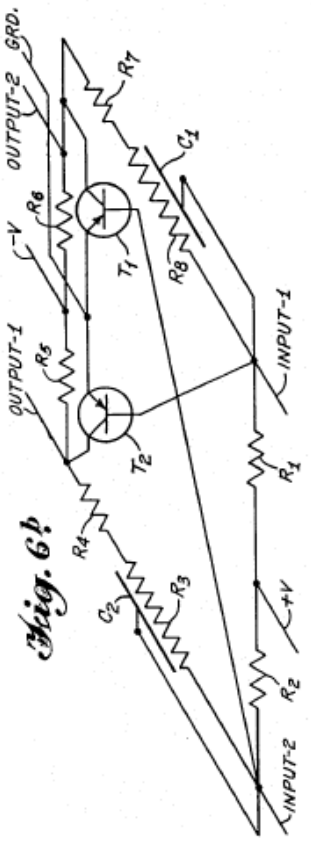

Fig. 6b.

INVENTOR

Jack S. Kilby

BY Stevens, Davis, Miller & Mosher

ATTORNEYS

United States Patent BEST AVAILABLE COPY [15] 3,643,138
Kilby [45] **Feb. 15, 1972**

[54] SEMICONDUCTOR DEVICE

[72] Inventor: **Jack St. Clair Kilby, Dallas, Tex.**

[73] Assignee: **Texas Instruments Incorporated, Dallas, Tex.**

[22] Filed: **Jan. 29, 1962**

[21] Appl. No.: **169,557**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 791,602, Feb. 6, 1959, Pat. No. 3,138,743, and a continuation-in-part of 811,476, May 6, 1959, abandoned, and a continuation-in-part of 811,486, May 6, 1959, Pat. No. 3,138,744.

[52] **U.S. Cl.** **317/235**, 317/234, 317/101
[51] **Int. Cl.** **H01l 19/00**
[58] **Field of Search** 317/234, 235, 101, 231

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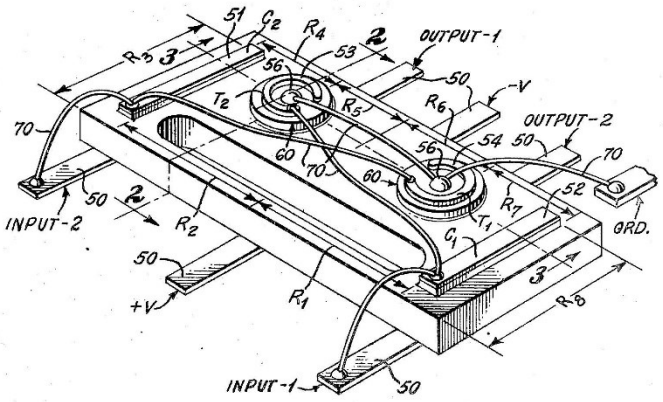
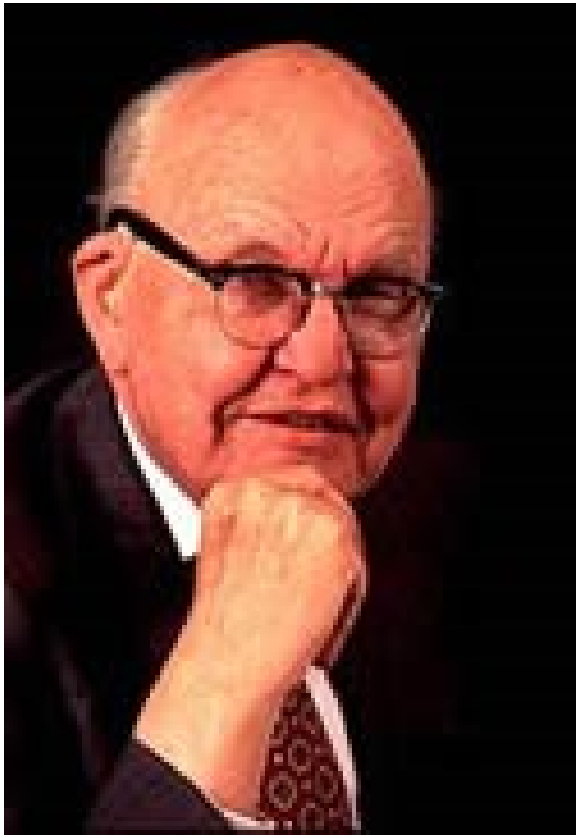
Primary Examiner—James D. Kallam
Attorney—James O. Dixon, Andrew M. Hassell, Robert C. Peterson and Stevens, Davis, Miller and Mosher

EXEMPLARY CLAIM

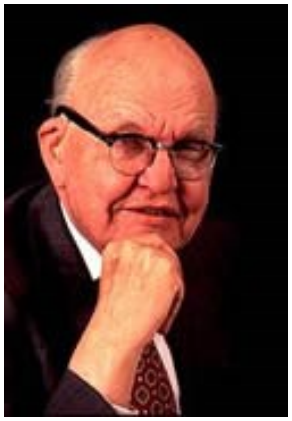
1. A semiconductor device comprising:
   a. a wafer of semiconductor material having two major faces;
   b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;
   c. at least some of said regions being electrically isolated within said wafer from others of said regions;
   d. said regions having at least one portion thereof extending to said one major face;
   e. at least some of said portions having selected locations on said one major face for electrical contact to said region;
   f. an insulating material on said one major face of the wafer excluding at least said selected locations;
   g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;
   h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component: and
   i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures

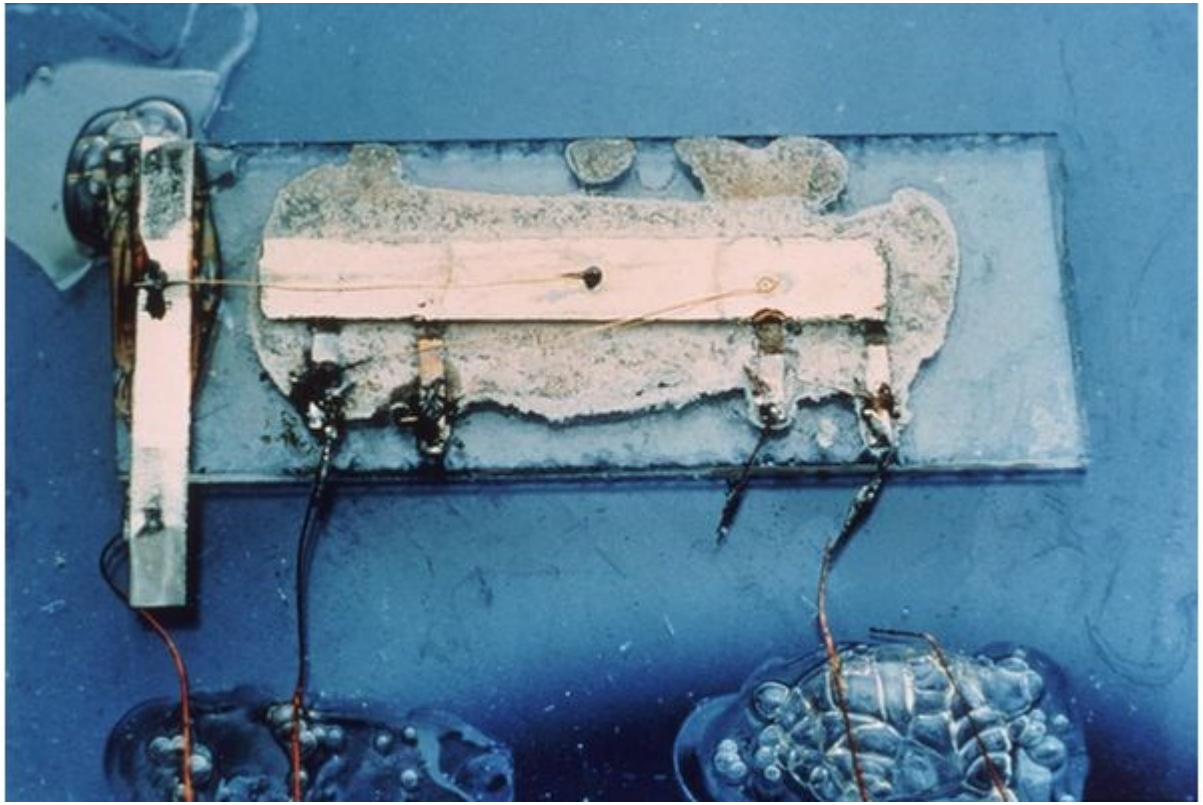




Jack Kilby



Jack Kilby



Kilby’s Integrated Circuit (germanium)

http://www.ti.com/corp/docs/kilbyctr/jackstclair.shtml

There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.

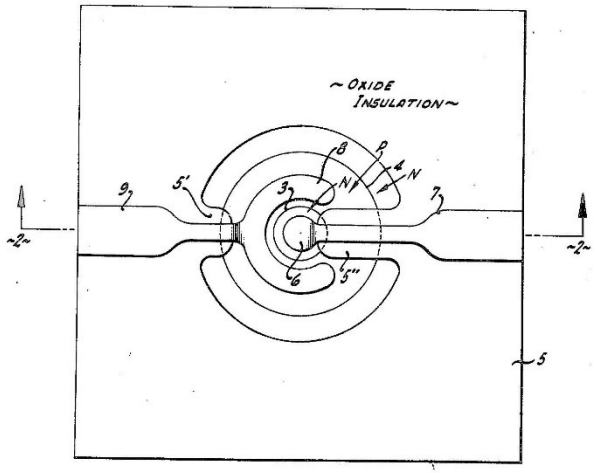
April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959

3 Sheets-Sheet 1

FIG-1



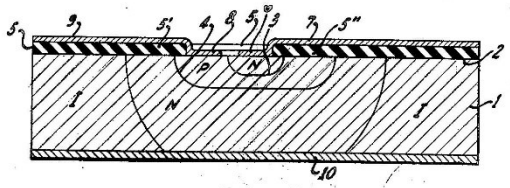


FIG-2

INVENTOR.
ROBERT N. NOYCE
BY Lieppincott & Ralls
ATTORNEYS

Robert Noyce

http://www.ideafinder.com/history/inventors/noyce.htm

Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today's computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.

While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.

After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel.

At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.

The key patents that revolutionized the electronics field:

Jack Kilby (34 years old at invention) patent: 3,138,743

Filed Feb 6, 1959 Issued June 23, 1964

Robert Noyce (31 years old at invention) patent: 2,981,877

Filed July 30, 1959 Issued April 25, 1961

Key Historical Developments

- 1971 Intel Introduces 4004 microprocessor (2300 transistors, 10u process)

Silicon Gate MOS **4004**

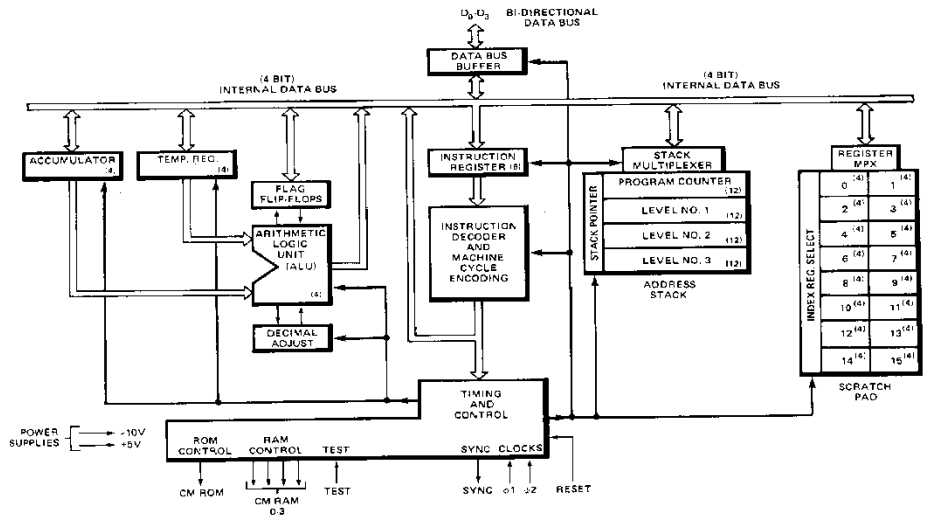
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **10.8 Microsecond Instruction Cycle**
- **CPU Directly Compatible With MCS-4 ROMs and RAMs**
- **Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM**
- **4-Bit Parallel CPU With 46 Instructions**
- **Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching**
- **Binary and Decimal Arithmetic Modes**

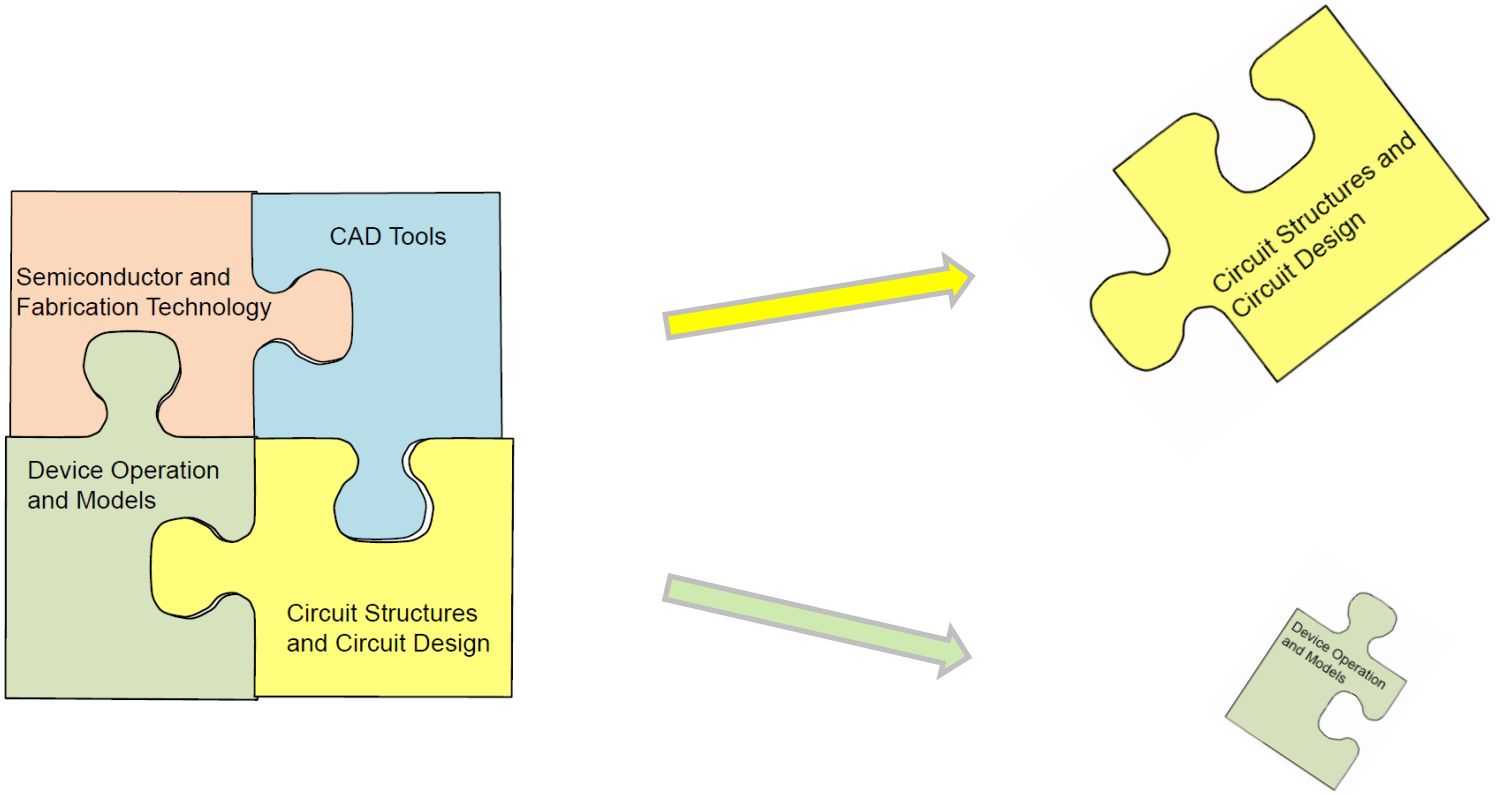
The Intel®4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



Basic Logic Circuits



Basic Logic Circuits

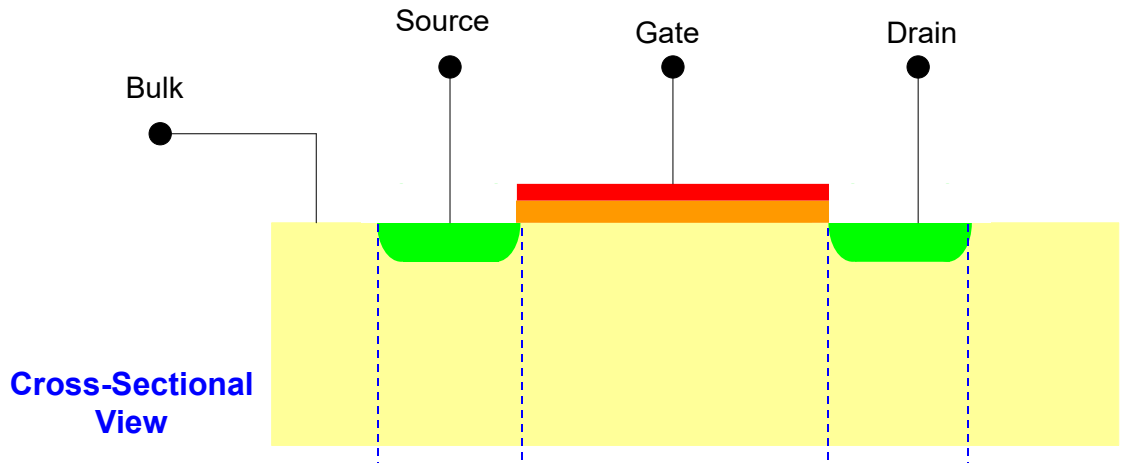
- Will present a brief description of logic circuits based upon simple models and qualitative description of processes
- Will later discuss process technology needed to develop better models
- Will even later provide more in-depth discussion of logic circuits based upon better device models

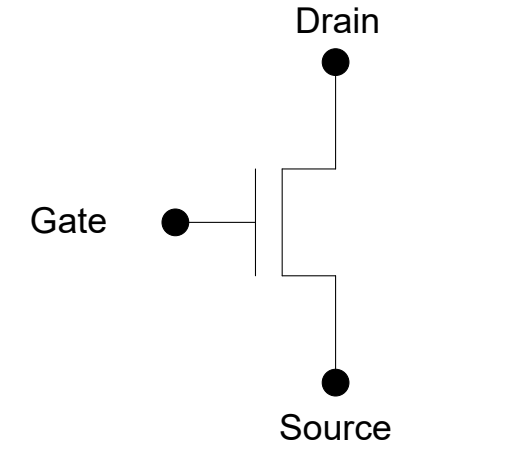
Models of Devices

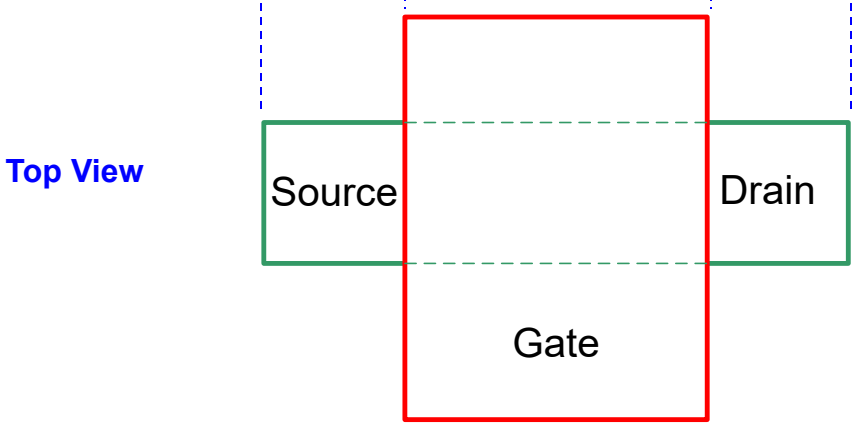
- Several models of the electronic devices will be introduced throughout the course
  - Complexity
  - Accuracy
  - Insight
  - Application
- Will use the simplest model that can provide acceptable results for any given application

MOS Transistor

Qualitative Discussion of n-channel Operation





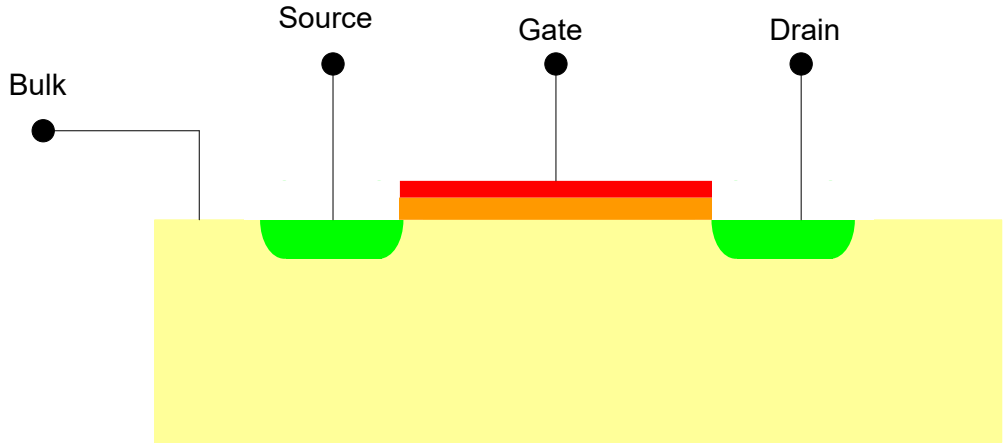


Designer always works with top view

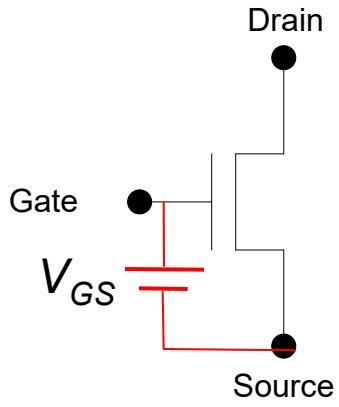
Complete Symmetry in construction between Drain and Source

MOS Transistor

Qualitative Discussion of n-channel Operation



n-channel MOSFET

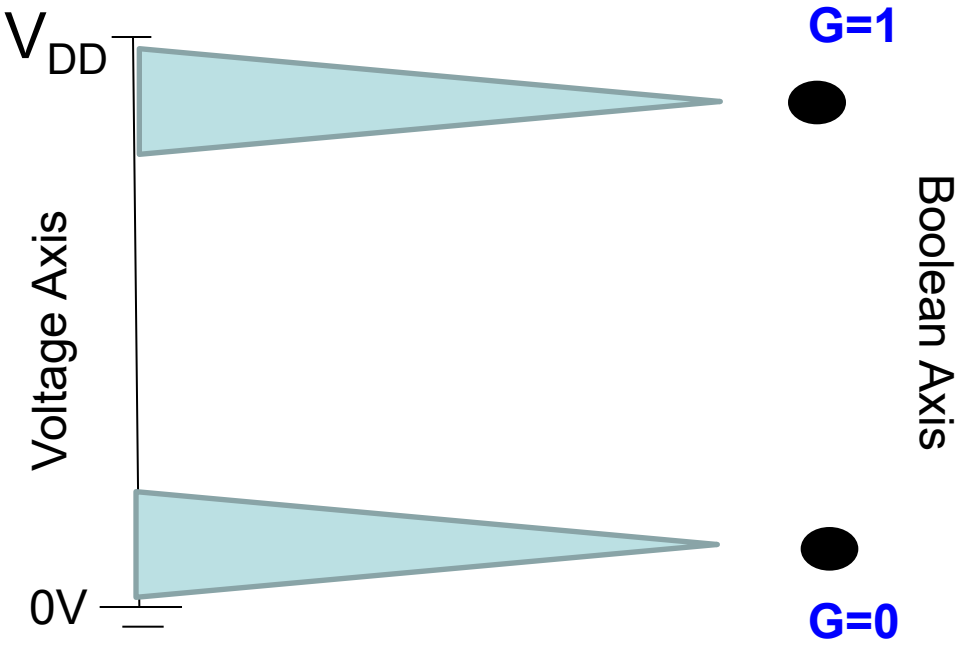


Behavioral Description of Operation of n-channel MOS Transistors Created for use in Basic Digital Circuits

If V_{GS} is large, short circuit exists between drain and source

If V_{GS} is small (or negative), open circuit exists between drain and source

Boolean/Continuous Notation:

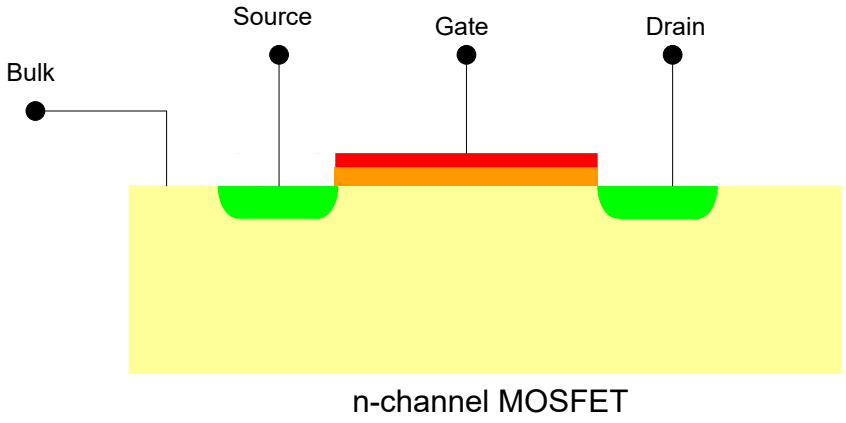


- **Voltage Axis is Continuous between 0V and V_{DD}**
- **Boolean axis is discrete with only two points**

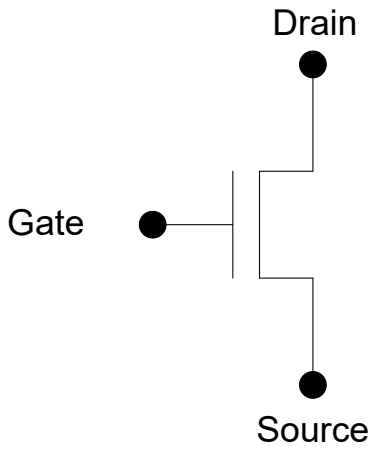
Most logic circuits characterized by the relationship between the Boolean input/output variables though these correspond to voltage intervals on the continuous voltage axis

MOS Transistor

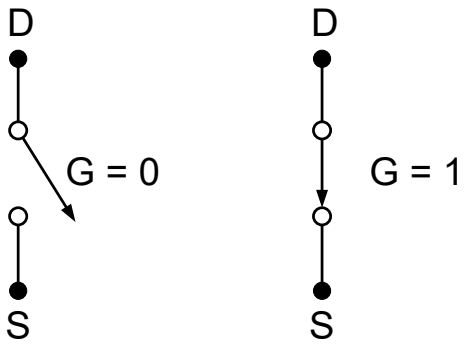
Qualitative Discussion of n-channel Operation



n-channel MOSFET



Equivalent Circuit for n-channel MOSFET



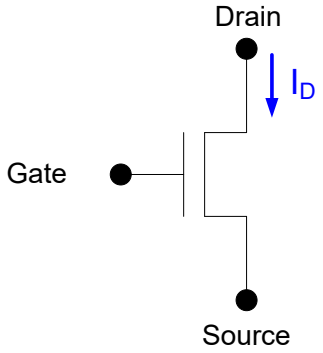
- V_{GS}=0 denoted as Boolean gate voltage G=0
- V_{GS}=V_{DD} denoted as Boolean gate voltage G=1

If source connected to (or close to) ground, Boolean G is relative to ground potential

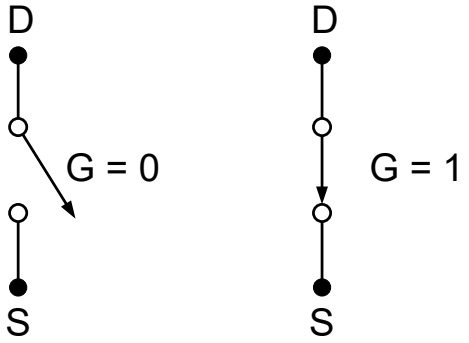
This is the first model we have for the n-channel MOSFET !

Ideal switch-level model

MOS Transistor MODEL



Equivalent Circuit for n-channel MOSFET with source at ground

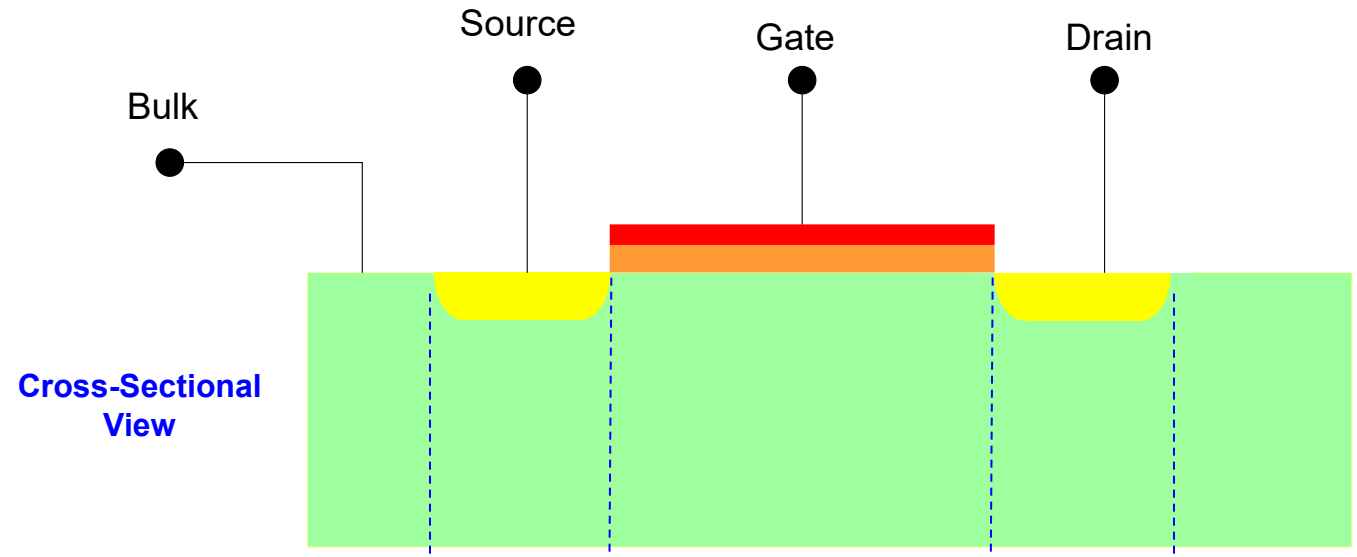


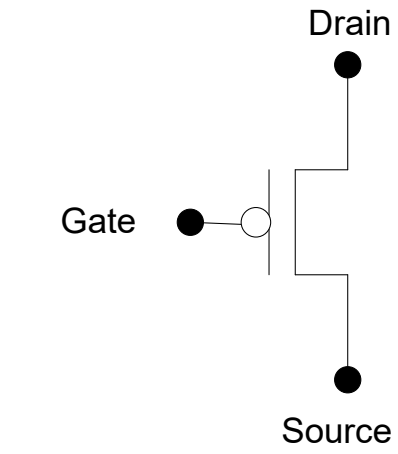
Mathematical model (not dependent upon Boolean notation):

$I_D = 0$	if V_{GS} is low (or negative)
$V_{DS} = 0$	if V_{GS} is high

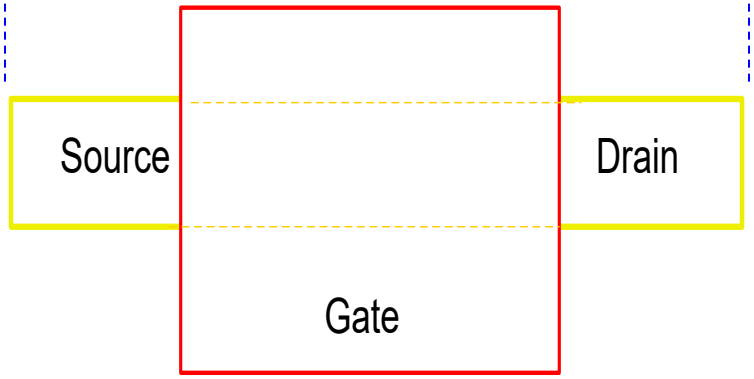
MOS Transistor

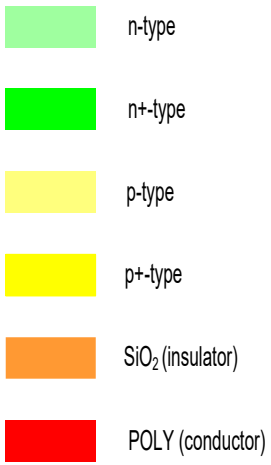
Qualitative Discussion of p-channel Operation





Symbol for p-channel MOSFET

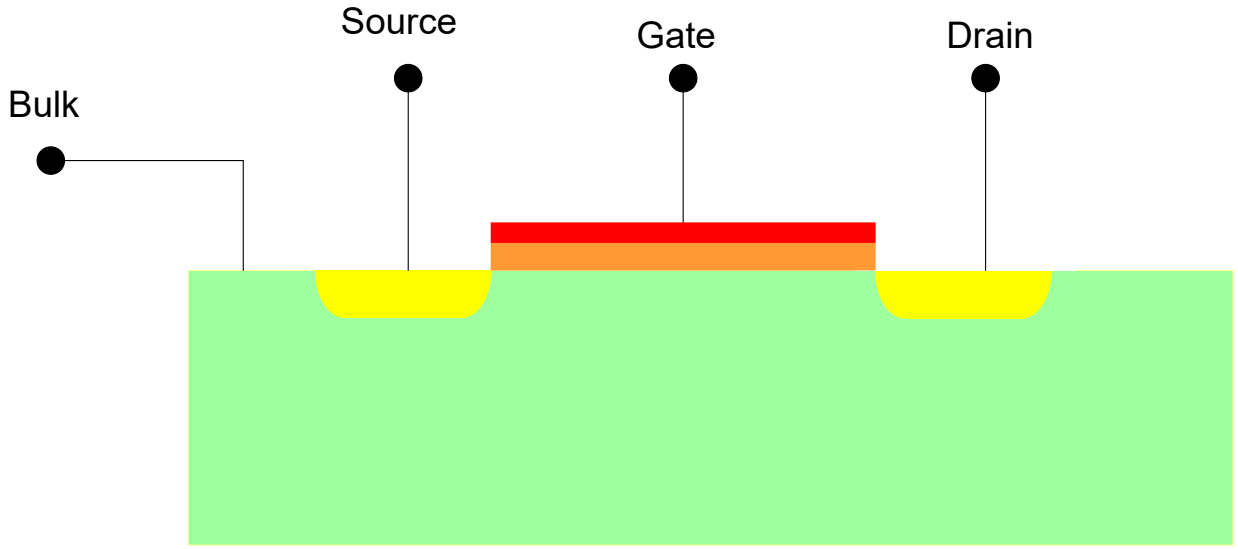


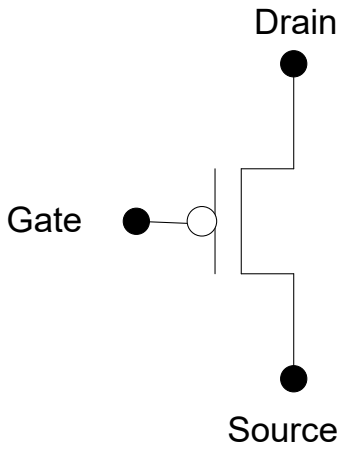


Complete Symmetry in construction between Drain and Source

MOS Transistor

Qualitative Discussion of p-channel Operation





p-channel MOSFET

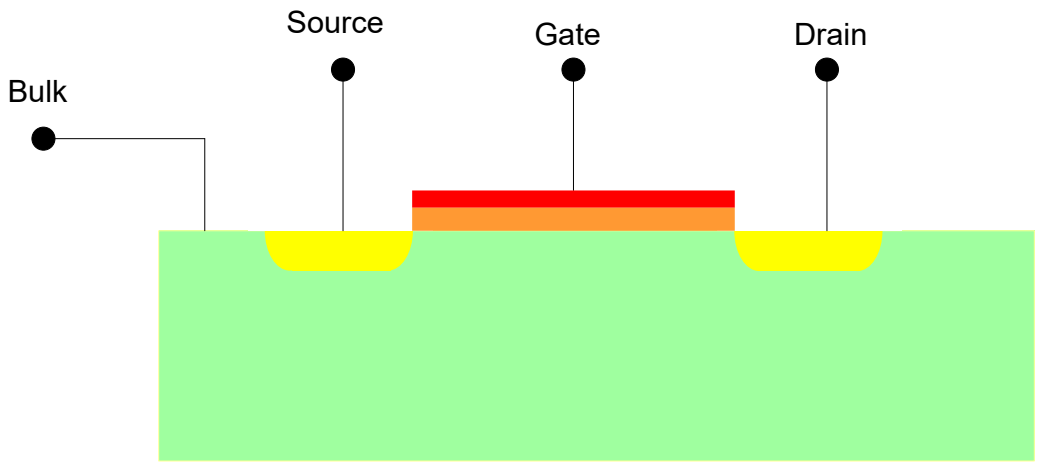
Behavioral Description of Operation of p-channel transistors created for use in basic digital circuits

If V_{GS} is large (and negative), short circuit exists between drain and source

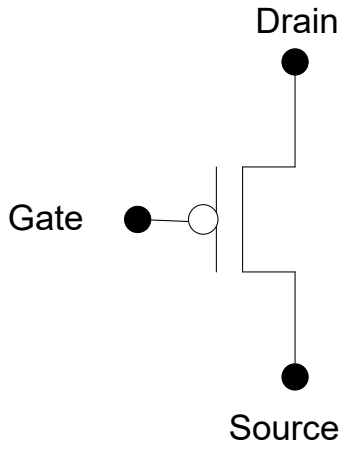
If V_{GS} is small (near 0 or positive), open circuit exists between drain and source

MOS Transistor

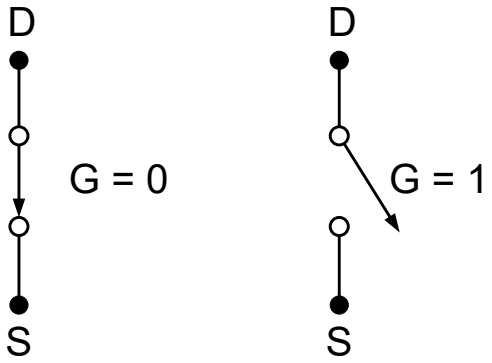
Qualitative Discussion of p-channel Operation



p-channel MOSFET



Equivalent Circuit for p-channel MOSFET

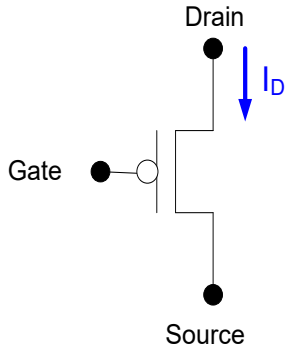


- For convenience assume Boolean G is relative to ground potential
- Assume Source connected to (or close to) positive V_{DD}

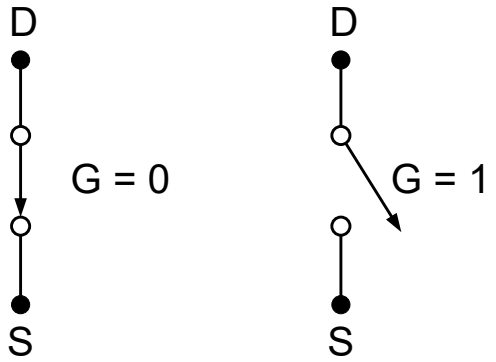
- V_{GS}=0 denoted as Boolean gate voltage G=1
- V_{GS}= -V_{DD} denoted as Boolean gate voltage G=0

This is the first model we have for the p-channel MOSFET !

MOS Transistor MODEL



Equivalent Circuit for p-channel MOSFET with Source at VDD

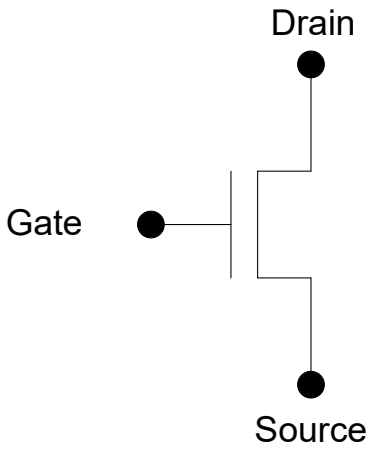


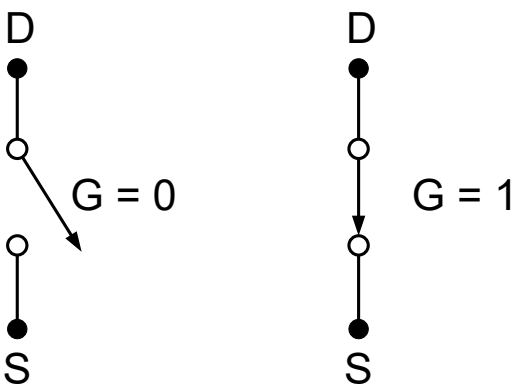
Mathematical model (not dependent upon Boolean notation):

$I_D = 0$	if $\lvert V_{GSp} \rvert$	is small or V_{GSp} is positive
$V_{DS} = 0$	if $\lvert V_{GSp} \rvert$	is large

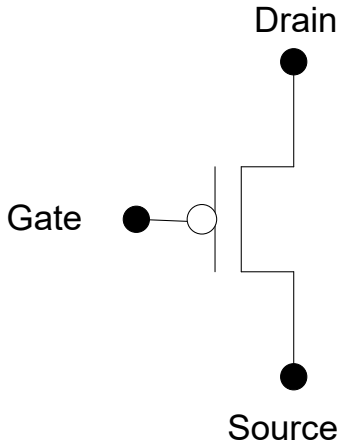
MOS Transistor

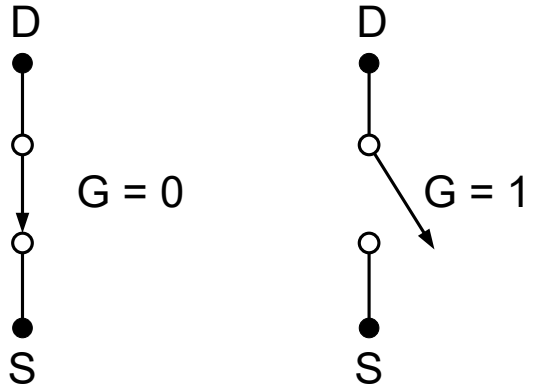
Comparison of Operation





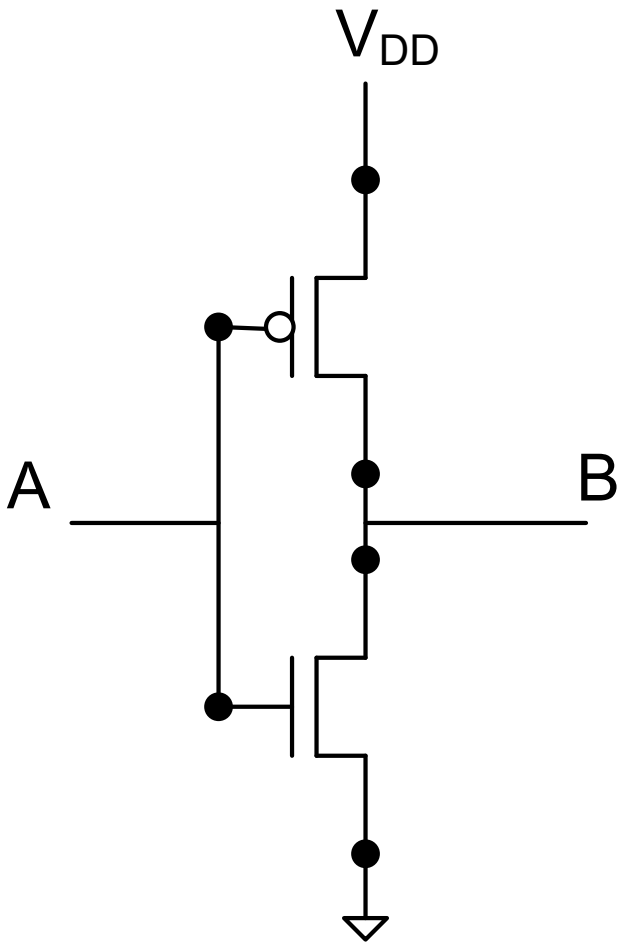
Source assumed connected to (or close to) ground

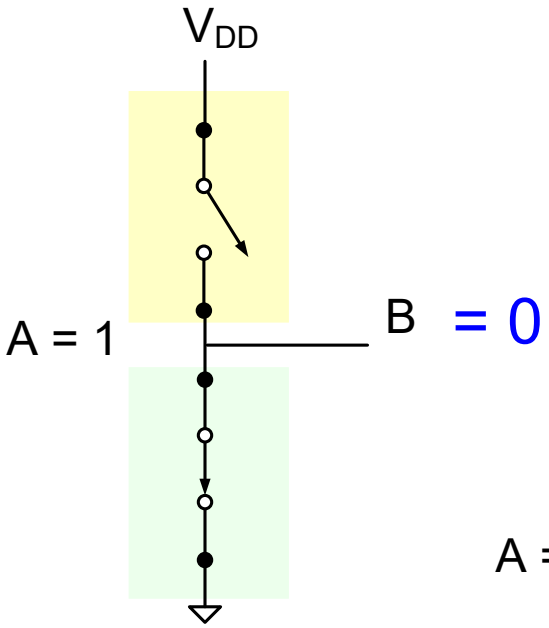


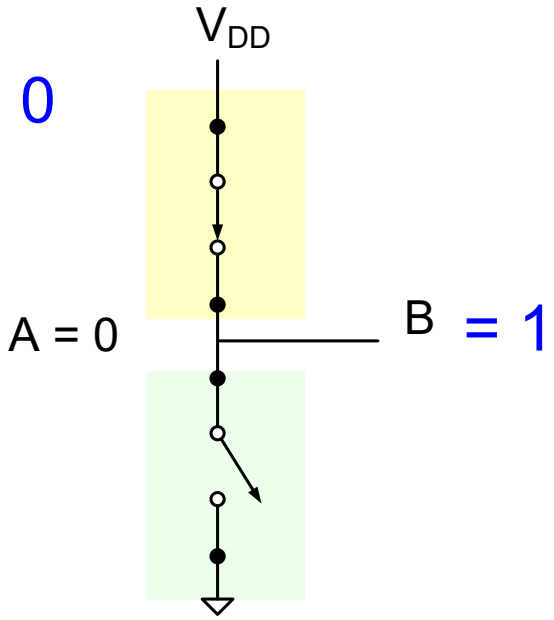


Source assumed connected to (or close to) positive V_{DD} and Boolean G at gate is relative to ground

Logic Circuits

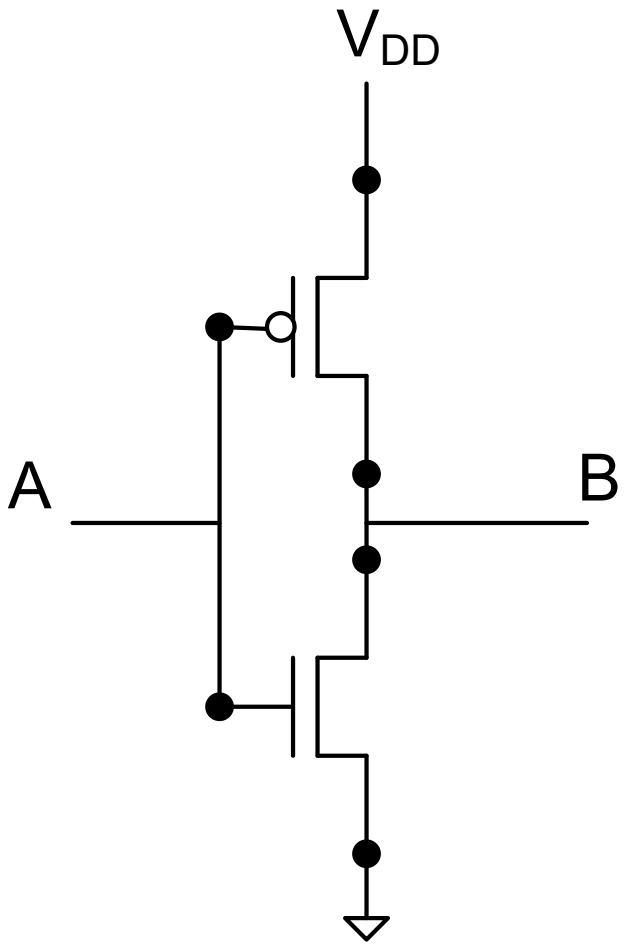






Circuit Behaves as a Boolean Inverter

Logic Circuits

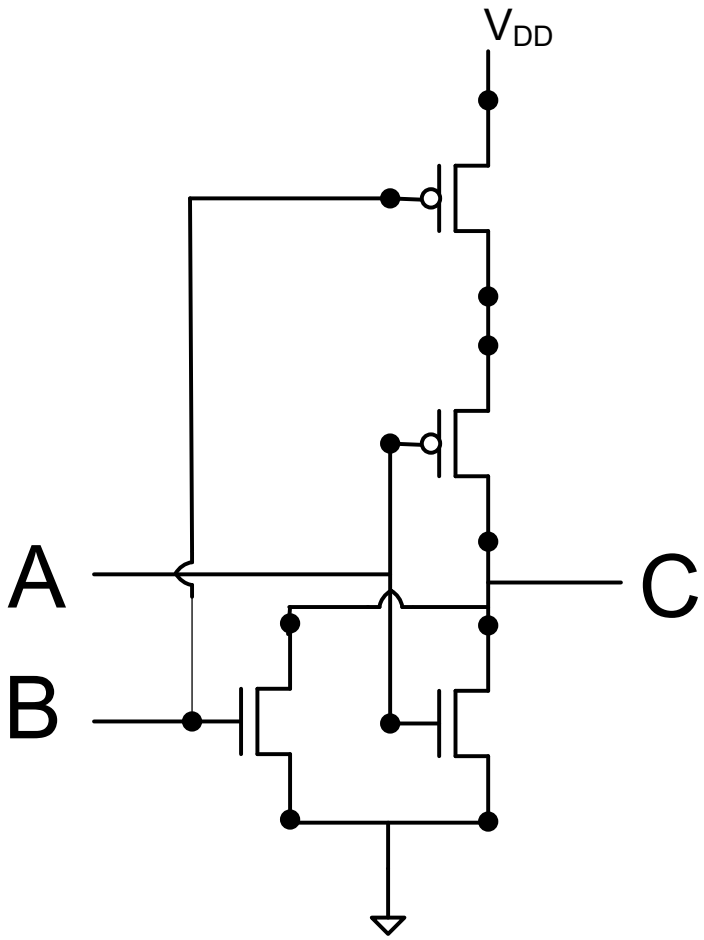


Truth Table

A	B
0	1
1	0

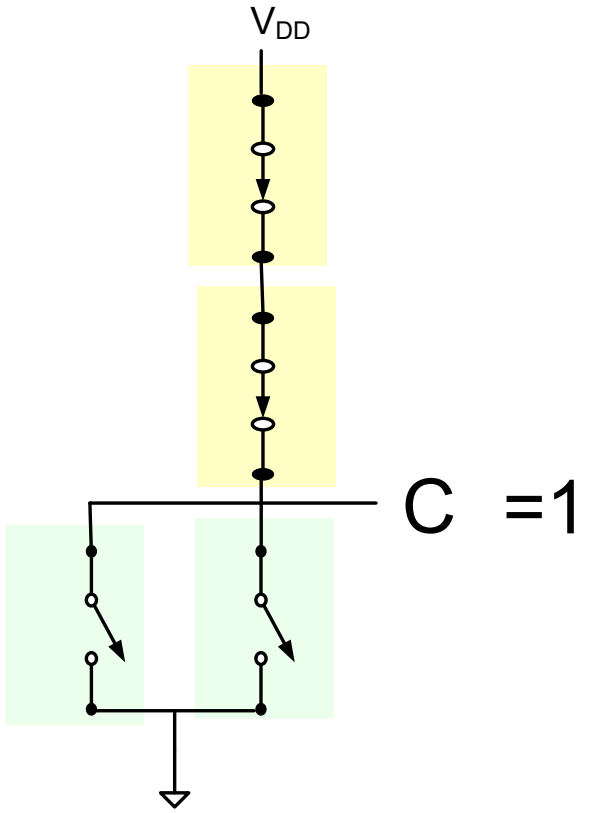
Inverter

Logic Circuits

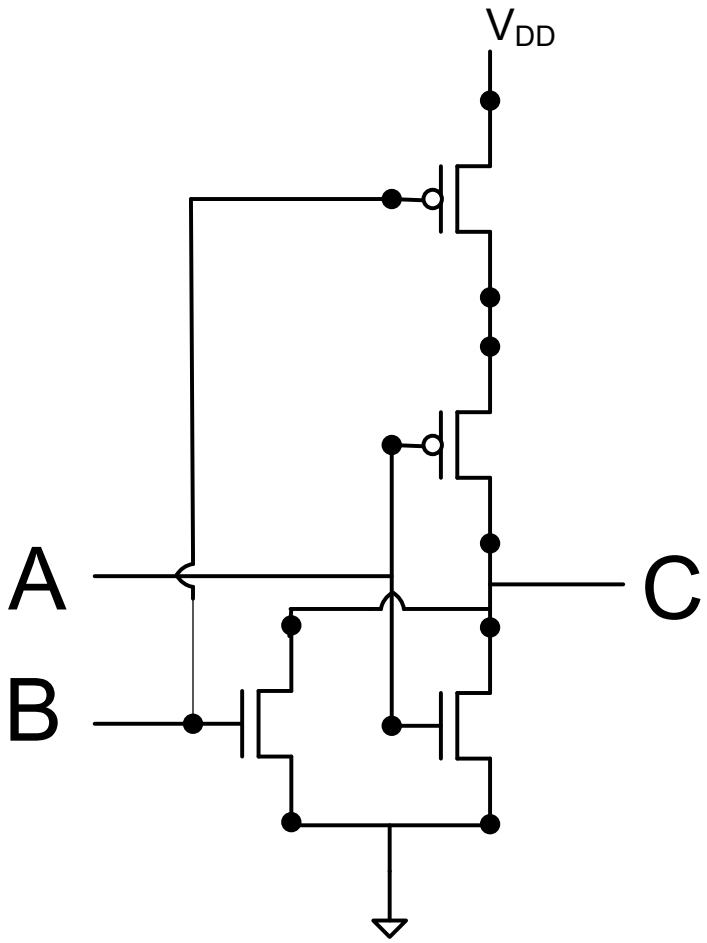


A=0

B=0

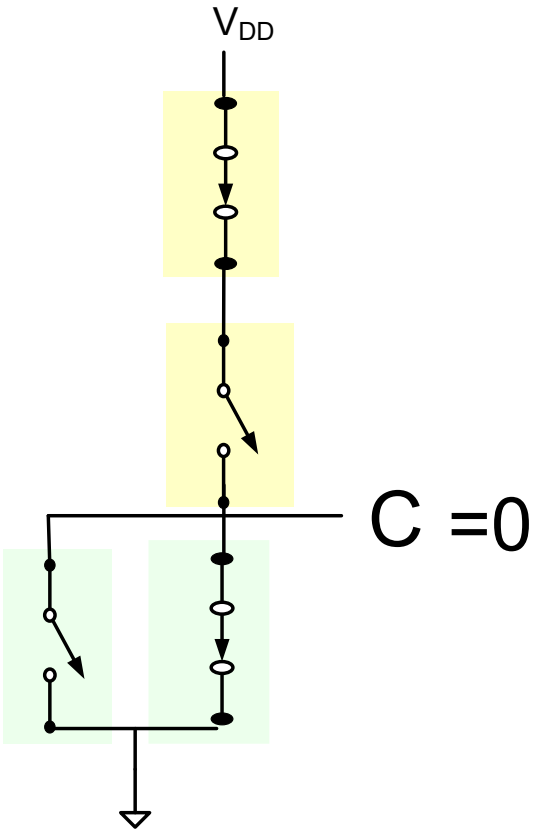


Logic Circuits

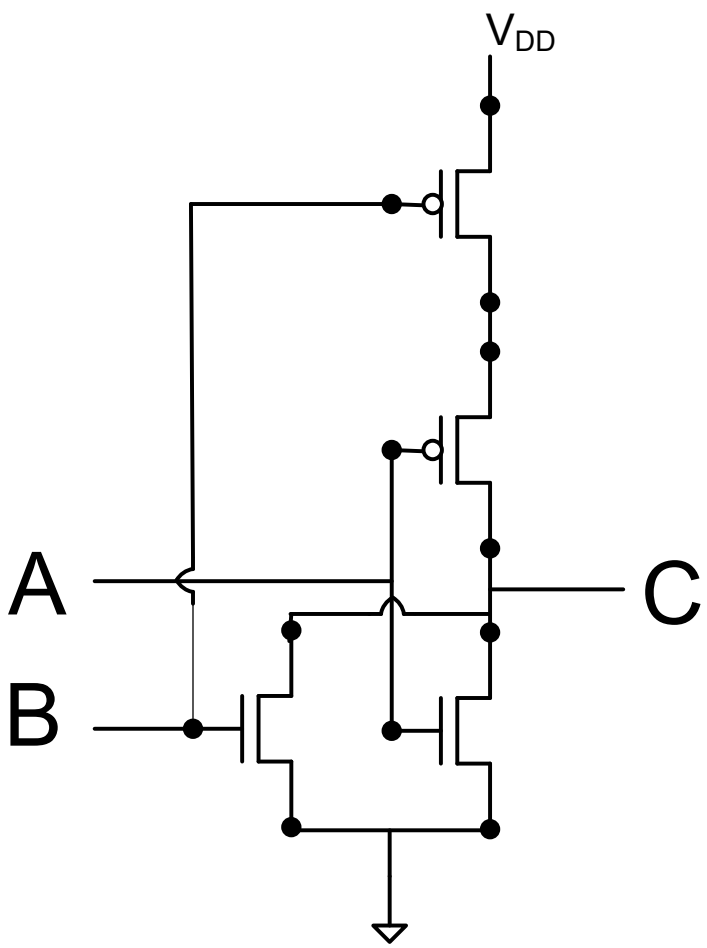


A=1

B=0

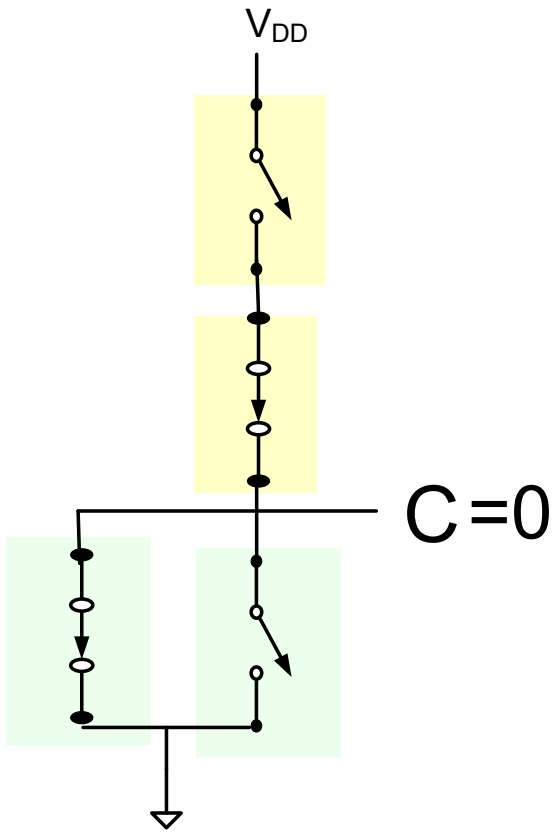


Logic Circuits

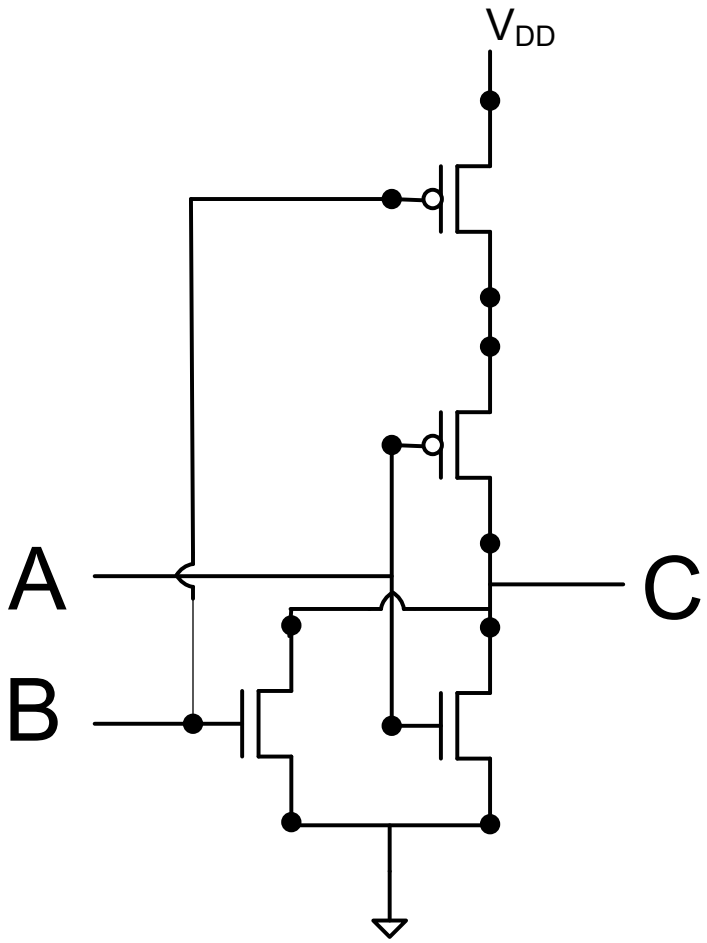


A=0

B=1

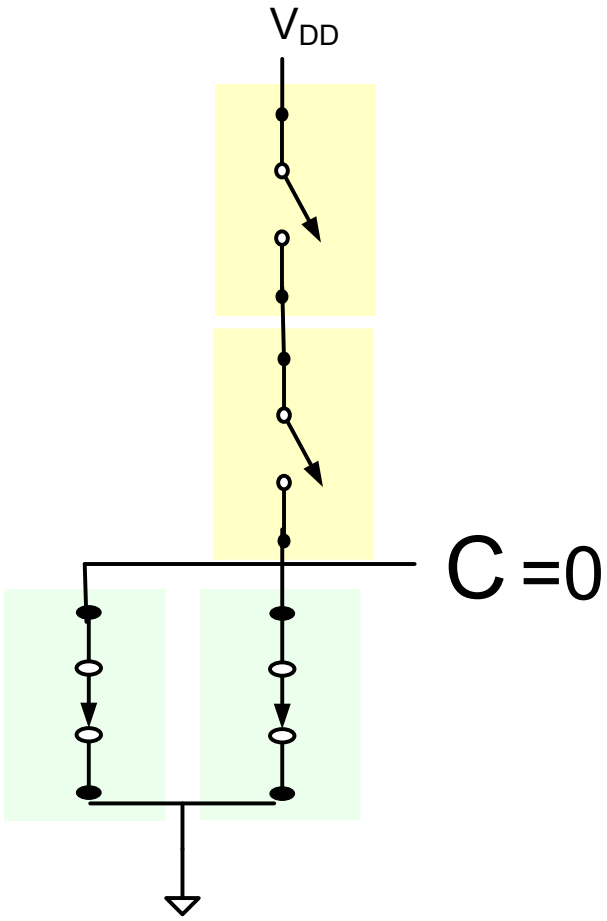


Logic Circuits

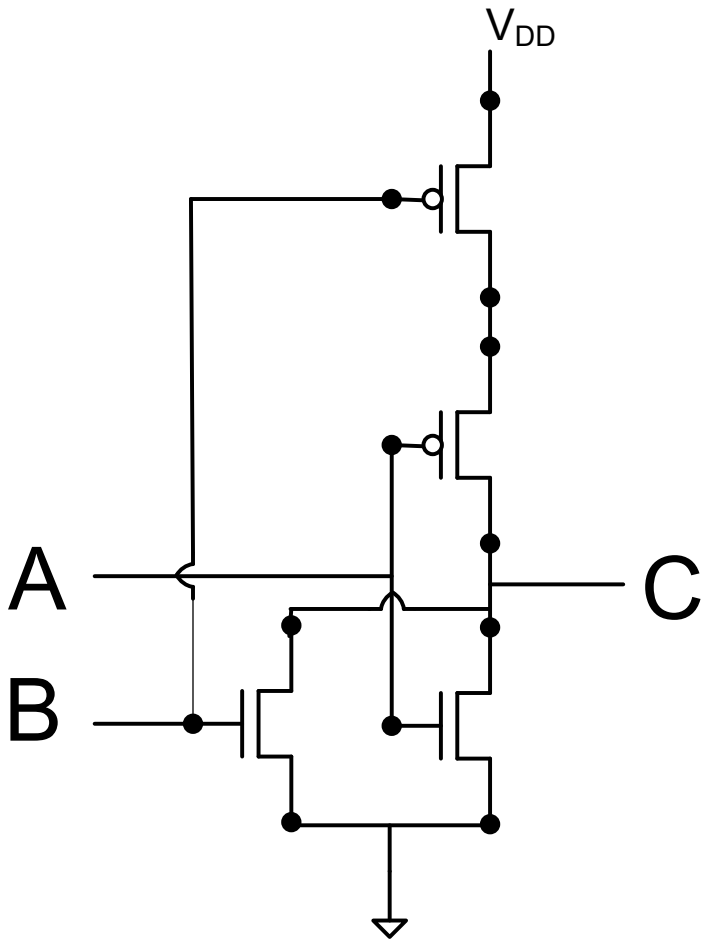


A=1

B=1



Logic Circuits

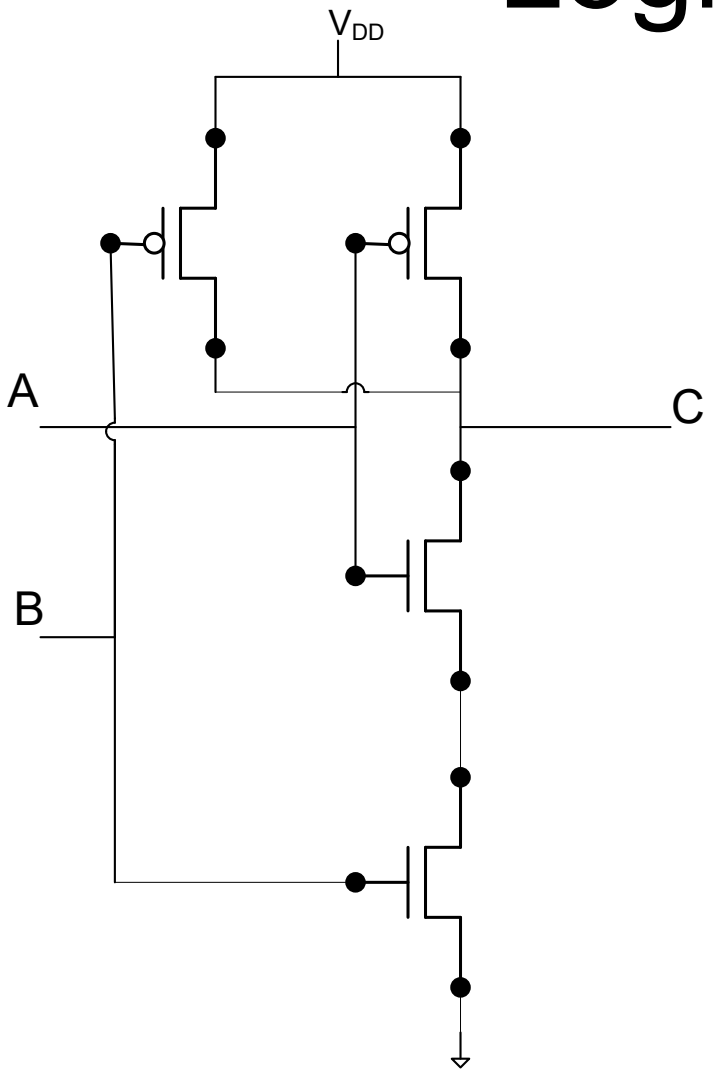


NOR Gate

Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Logic Circuits

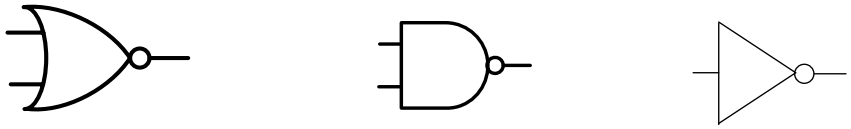


NAND Gate

Truth Table

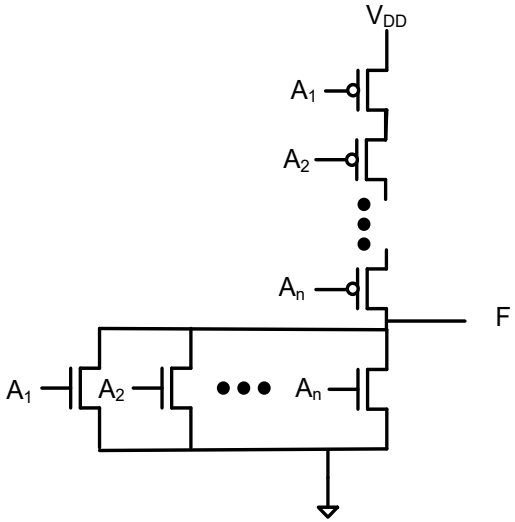
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

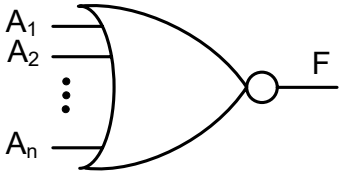
Logic Circuits



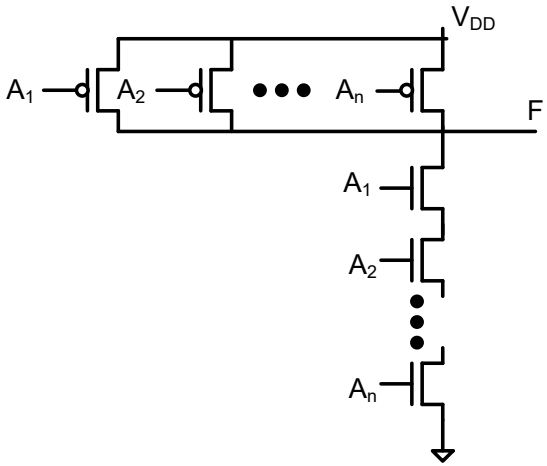
Approach can be extended to arbitrary number of inputs

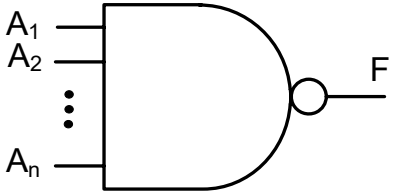
n-input NOR gate



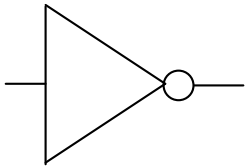


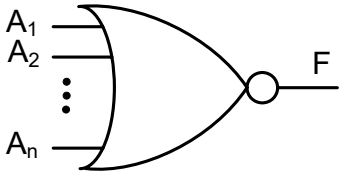
n-input NAND gate

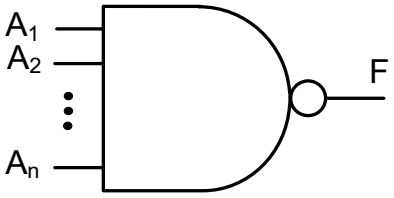




Complete Logic Family







Family of n-input NOR gates forms a complete logic family

Family of n-input NAND gates forms a complete logic family

Having both NAND and NOR gates available is a luxury

Can now implement any combinational logic function !!

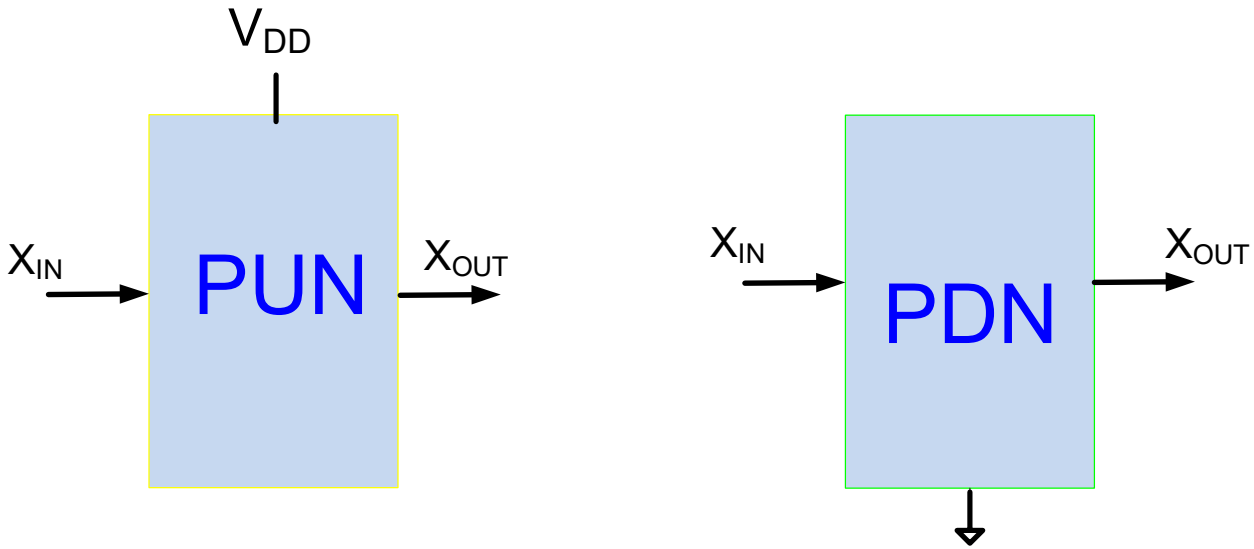
If add one flip flop, can implement any Boolean system !!

Flip flops easy to design but will discuss sequential logic systems later

Other logic circuits

- Other methods for designing logic circuits exist
- Insight will be provided on how other logic circuits evolve
- Several different types of logic circuits are often used simultaneously in any circuit design

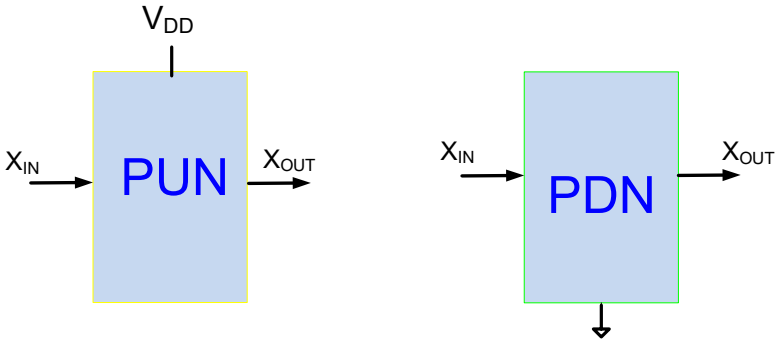
Pull-up and Pull-down Networks



- Pull-Up Network “pulls” output up to V_{DD} in response to some input X_{IN}

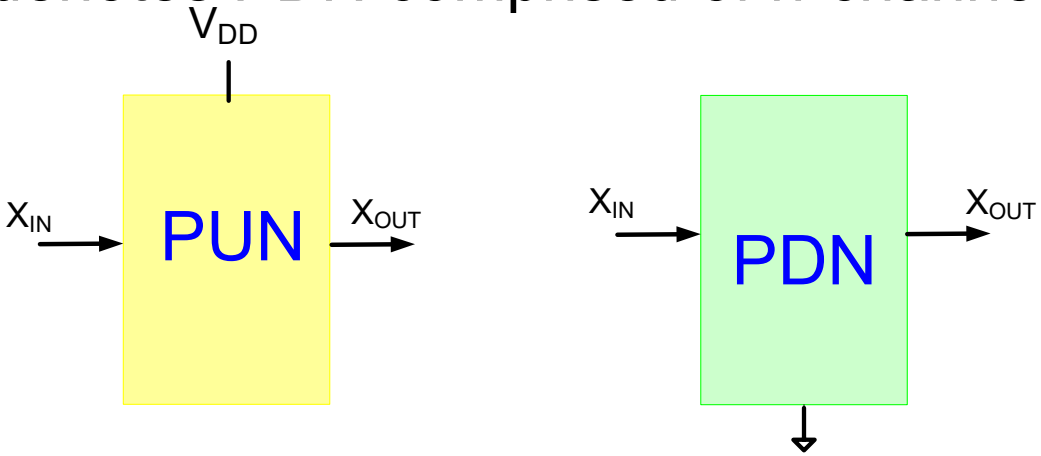
- Pull-Down Network “pulls” output down to ground in response to some input X_{IN}

Pull-up and Pull-down Networks

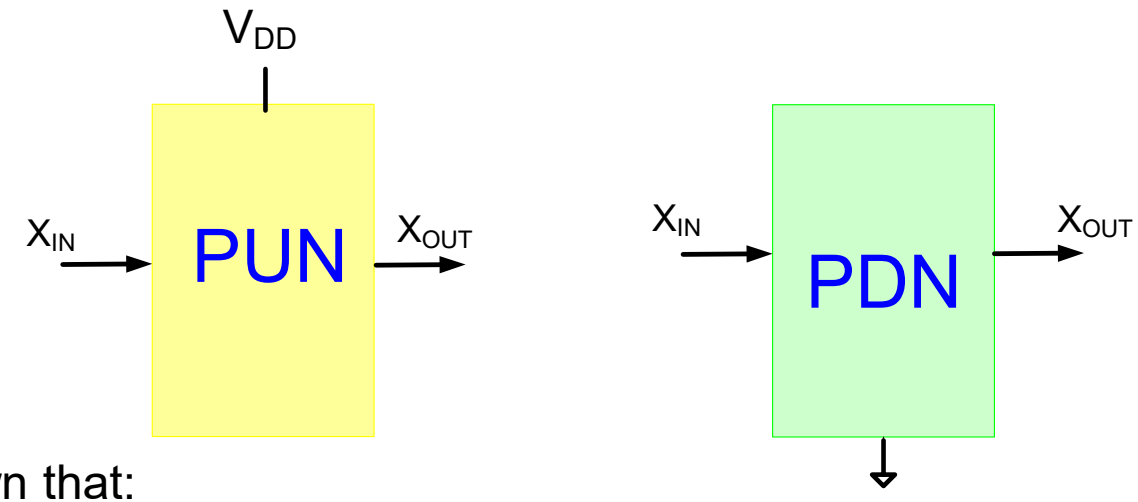


Color convention in following slides (and through much of course)

- Yellow denotes PUN comprised of p-channel devices
- Green denotes PDN comprised of n-channel devices



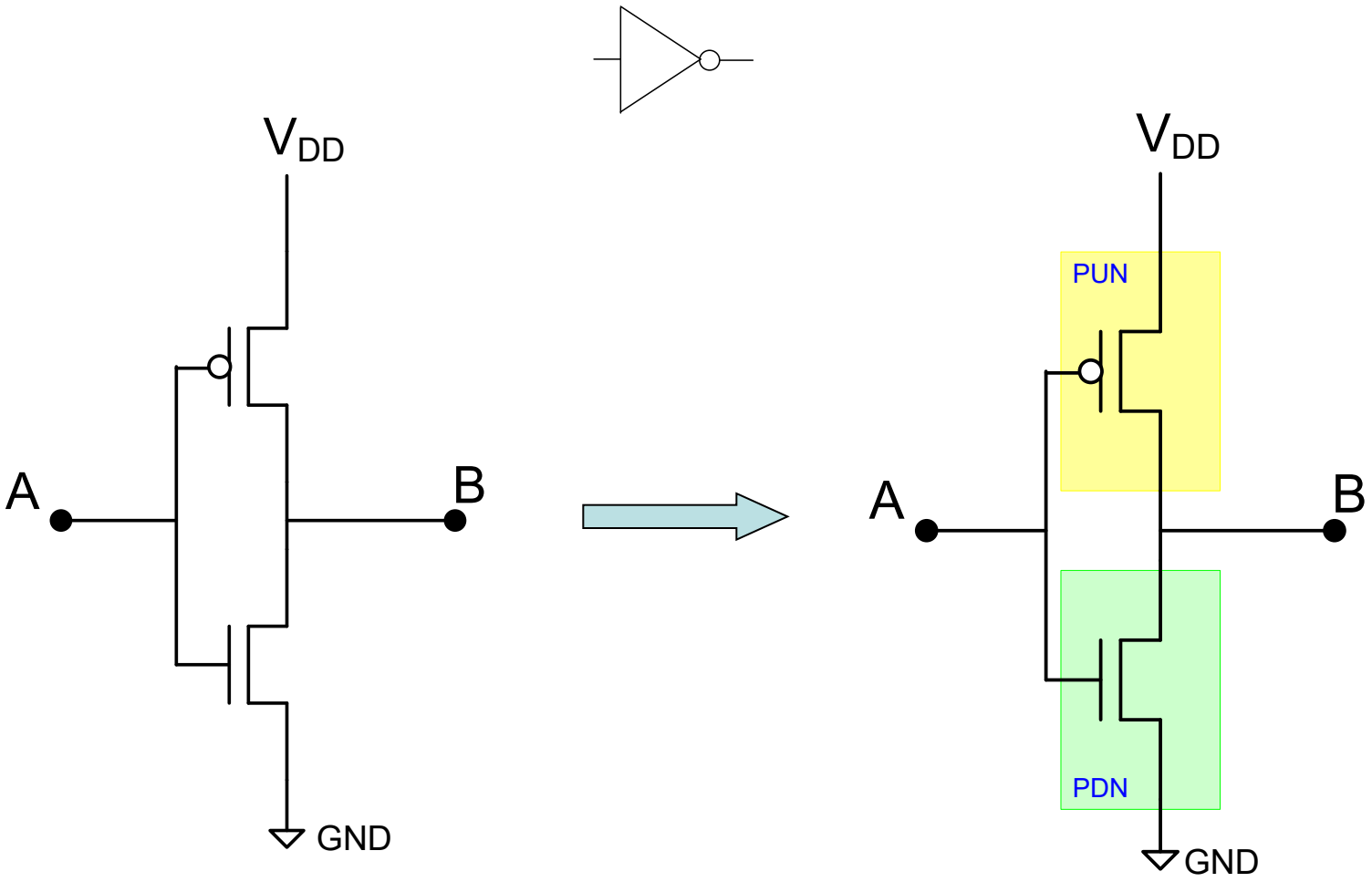
Pull-up and Pull-down Networks



It will be shown that:

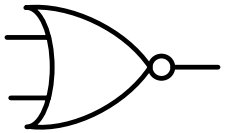
- Conduction is via electrons in n-channel devices and via holes in p-channel devices
- Logic circuits comprised entirely of p-channel PUNs and n-channel PDNs have some very attractive electrical properties

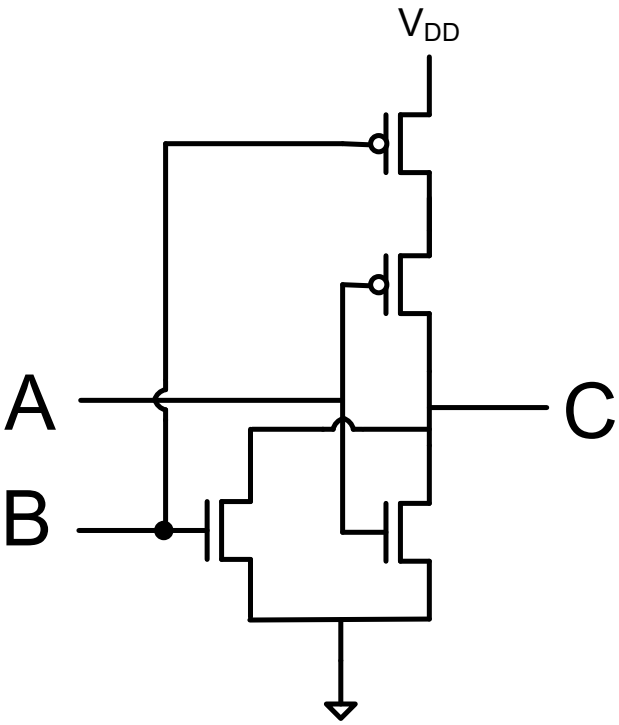
Pull-up and Pull-down Networks

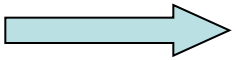


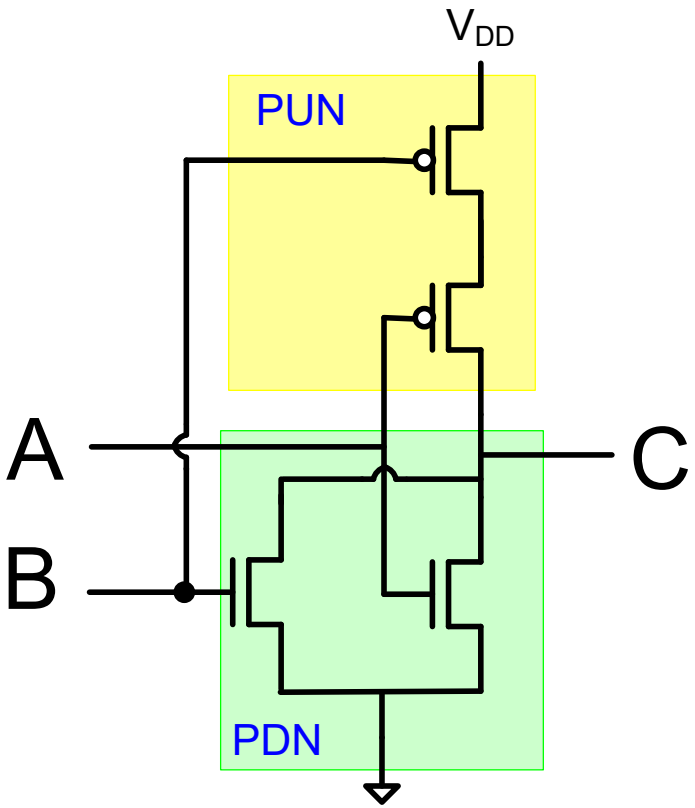
PU network comprised of p-channel device and “tries” to pull B to VDD when conducting
PD network comprised of n-channel device and “tries to pull B to GND when conducting
One and only one of these networks is conducting at the same time (to avoid contention)

Pull-up and Pull-down Networks



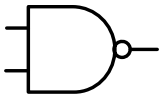


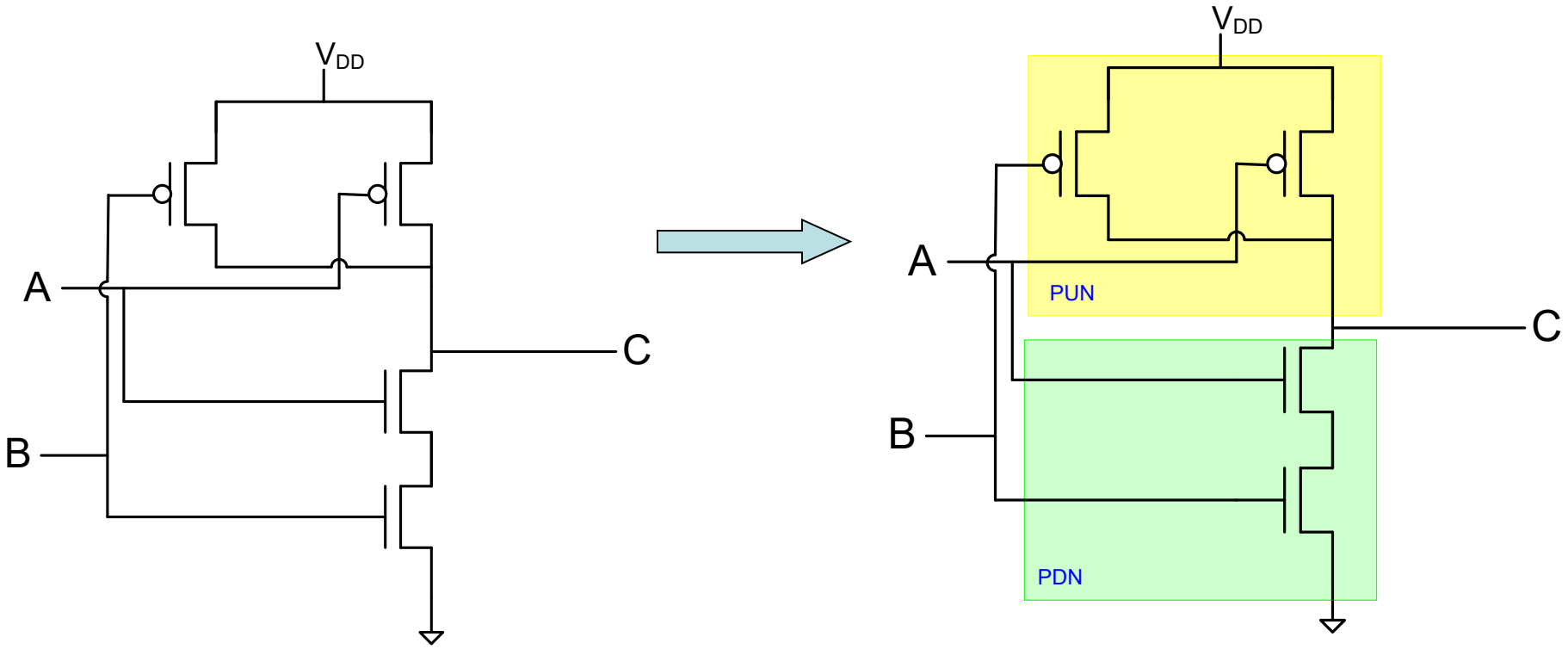




PU network comprised of p-channel devices
PD network comprised of n-channel devices
One and only one of these networks is conducting at the same time

Pull-up and Pull-down Networks





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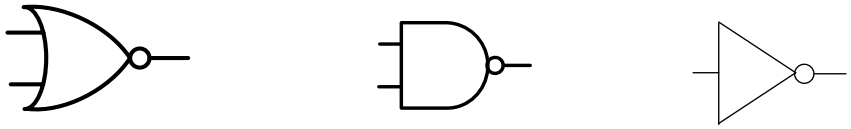
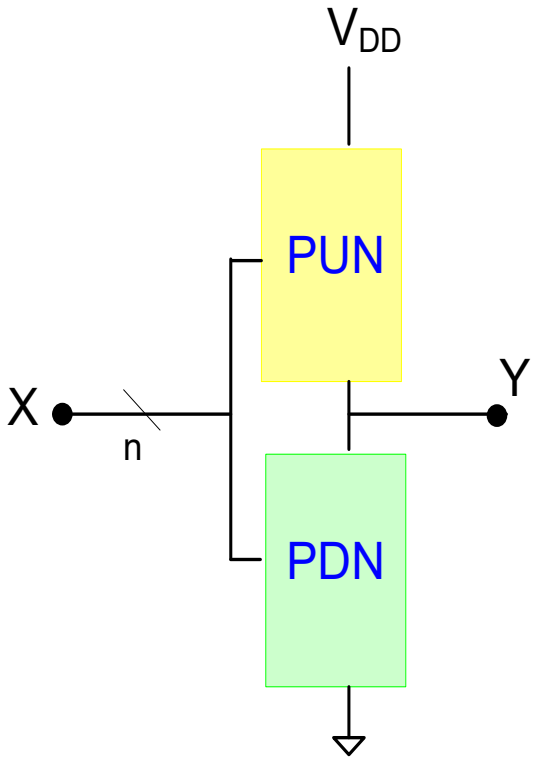
Pull-up and Pull-down Networks



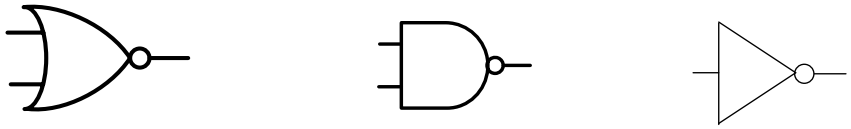
In these circuits, the PUN and PDN have the 3 interesting characteristics

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time



What are V_H and V_L?
What is the power dissipation?
How fast are these logic circuits?

Pull-up and Pull-down Networks



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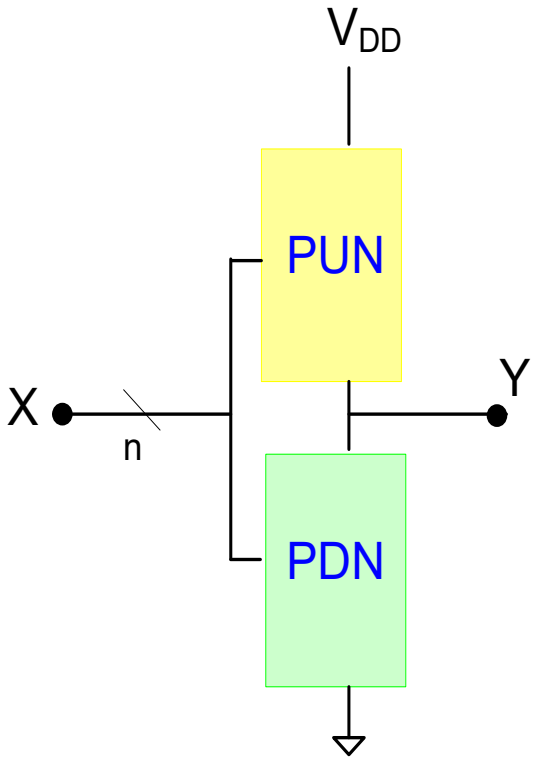

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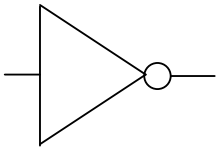
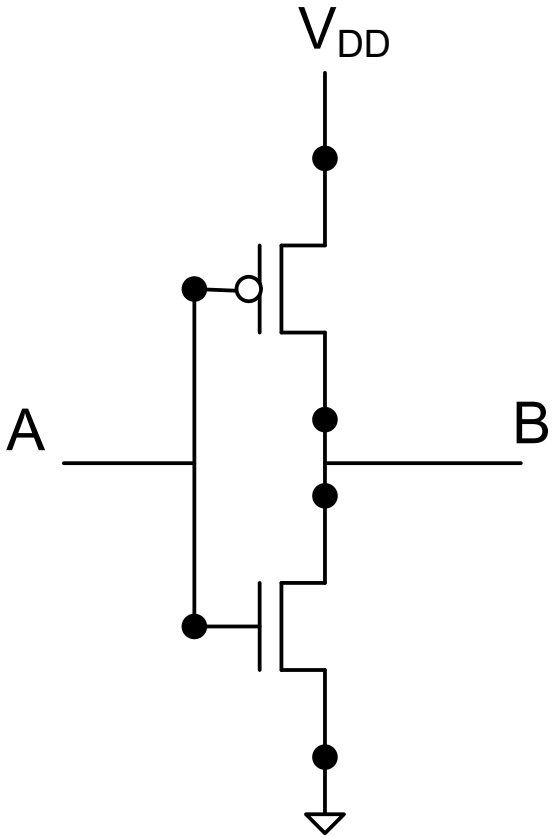
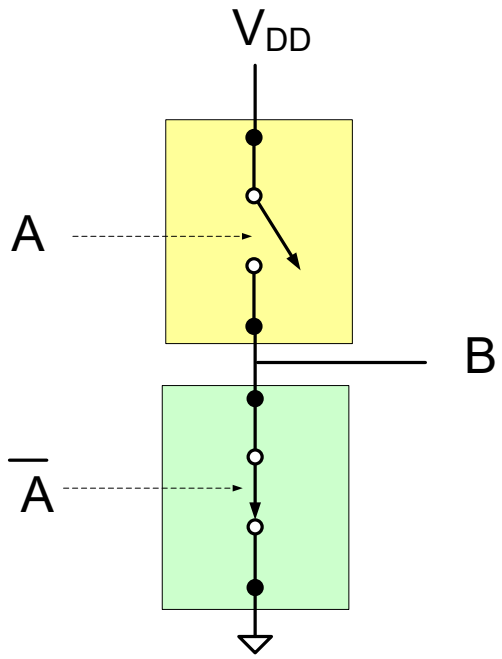
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices







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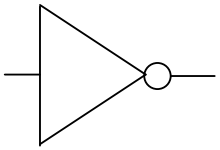
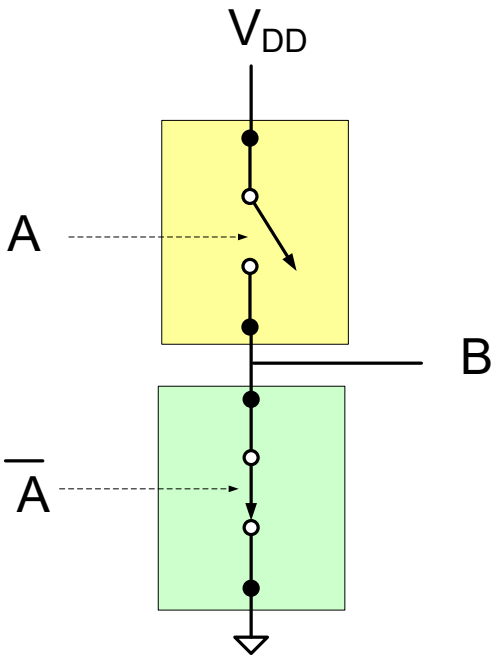




$V_H=V_{DD}$

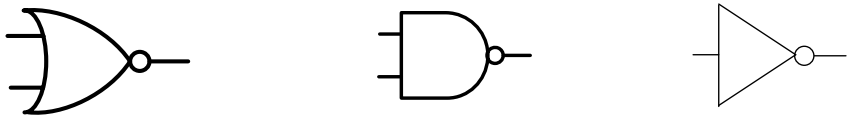
$V_L=0$

$I_D=0$ thus $P_H=P_L=0$

$t_{HL}=t_{LH}=0$

(too good to be true?)

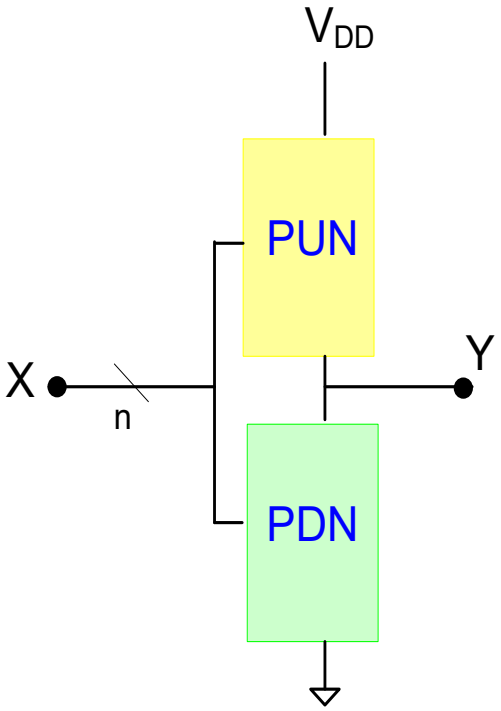
Pull-up and Pull-down Networks



For these circuits, the PUN and PDN have 3 interesting characteristics

Three key characteristics of these Static CMOS Gates

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time



Three key properties of these Static CMOS Gates

(assuming ideal switch-level device models)

1. What are V_H and V_L?

   $V_H=V_{DD}$, $V_L=0$ (too good to be true?)
2. What is the power dissipation?

   $P_H=P_L=0$ (too good to be true?)
3. How fast are these logic circuits?

   $t_{HL}=t_{LH}=0$ (too good to be true?)

These 3 properties inherent in all Boolean circuits with these 3 characteristics

(provided the ideal switch-level model is used for the transistors)

Pull-up and Pull-down Networks

Three key characteristics of Static CMOS Gates

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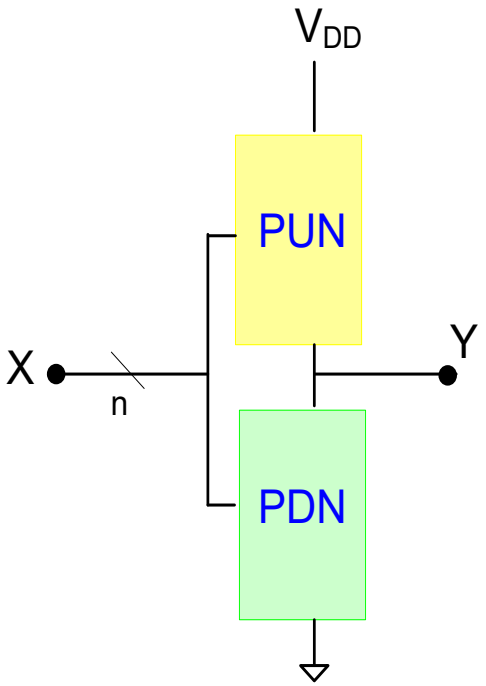

Three properties of Static CMOS Gates
(based upon simple switch-level model)

1. $V_H=V_{DD}$, $V_L=0$ (too good to be true?)
2. $P_H=P_L=0$ (too good to be true?)
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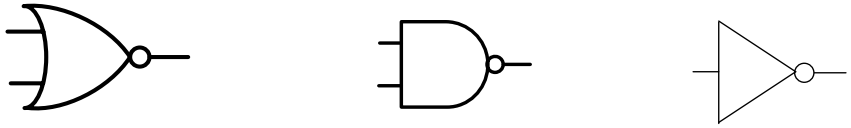
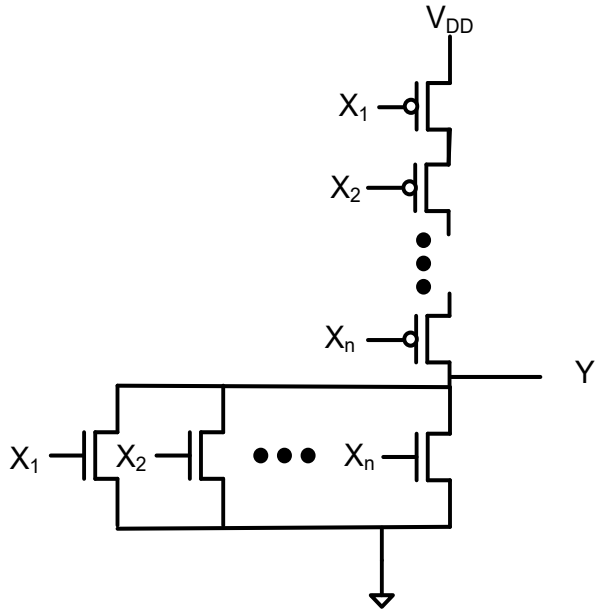
Pull-up and Pull-down Networks

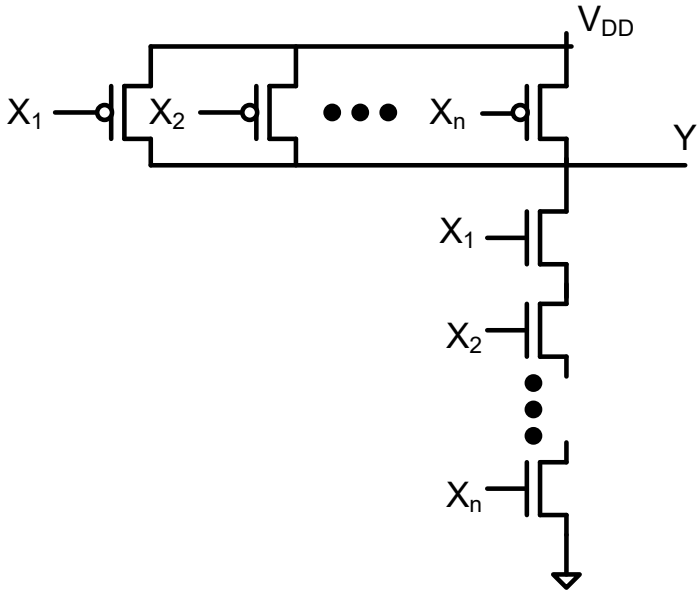


Thus, concept can be extended to arbitrary number of inputs

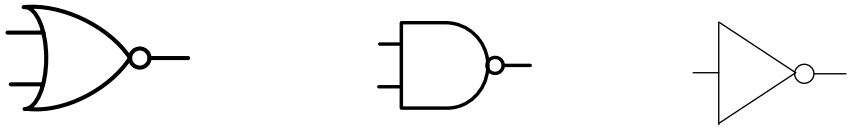
n-input NOR gate



n-input NAND gate



Pull-up and Pull-down Networks



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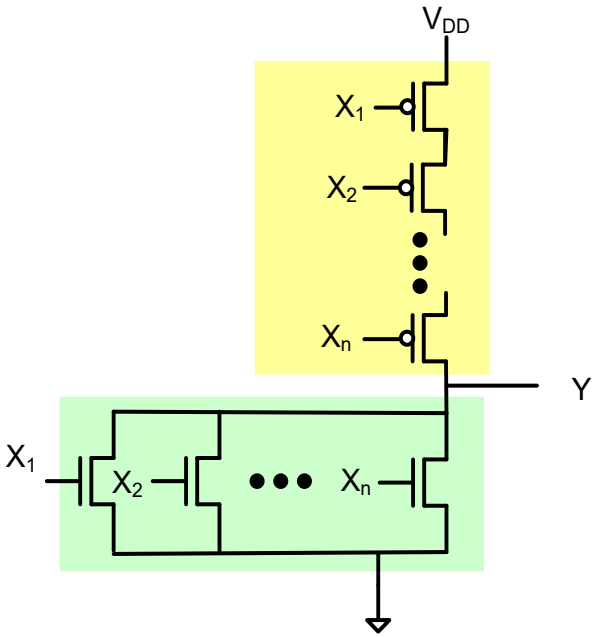

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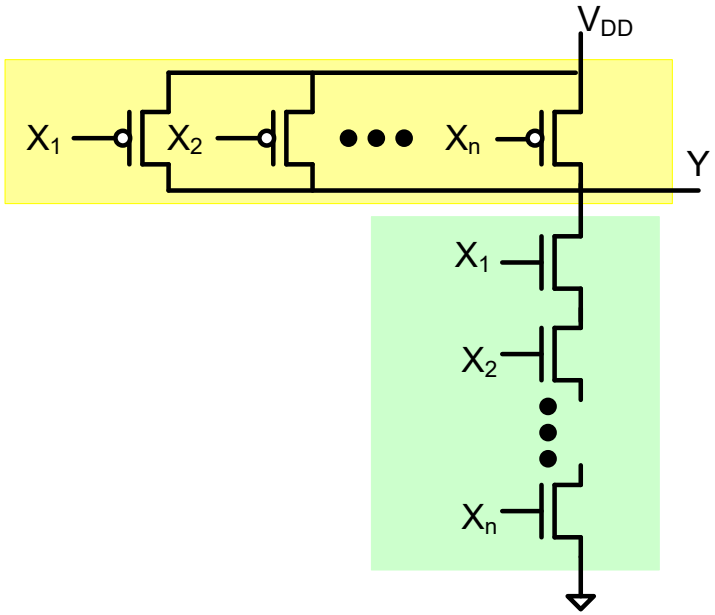

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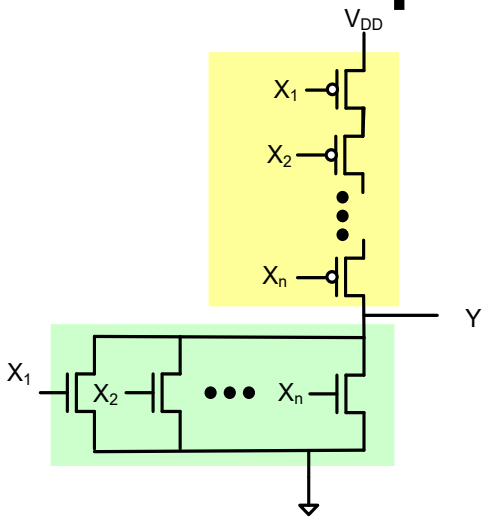
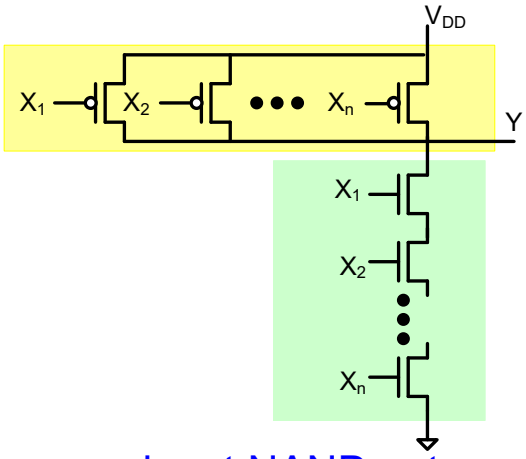
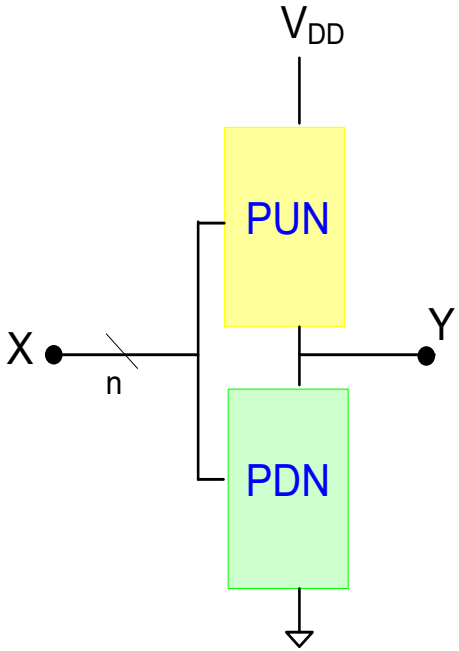
Pull-up and Pull-down Networks



n-input NOR gate



n-input NAND gate



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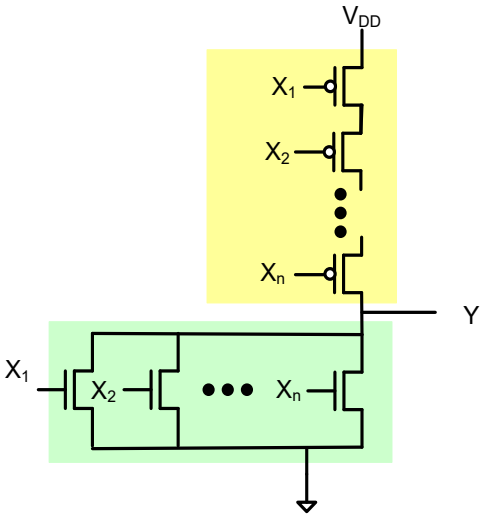
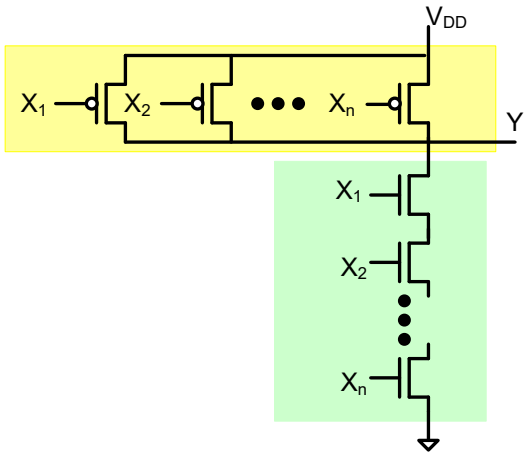
Nomenclature



n-input NOR gate



n-input NAND gate

In this class, logic circuits that are implemented by interconnecting multiple-input NAND and NOR gates will be referred to as "Static CMOS Logic"

Since the set of NAND gates is complete, any combinational logic function can be realized with the NAND circuit structures considered thus far

Since the set NOR gates is complete, any combinational logic function can be realized with the NOR circuit structures considered thus far

Many logic functions are realized with "Static CMOS Logic" and this is probably the dominant design style used today!

Stay Safe and Stay Healthy !

End of Lecture 5